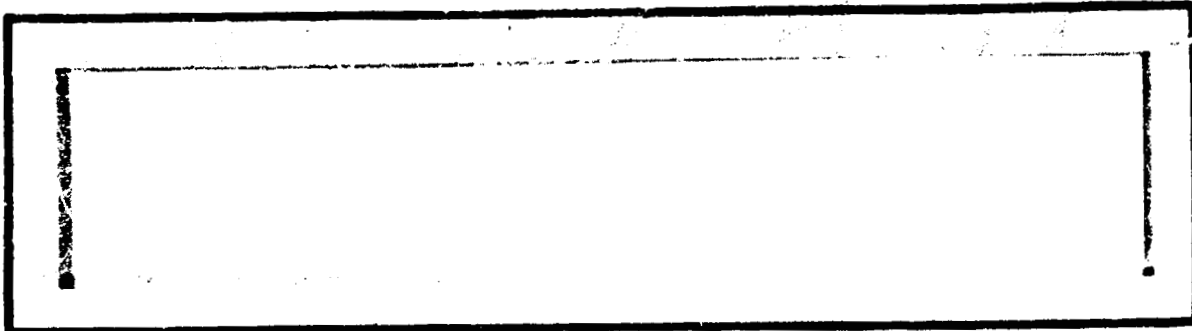


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(NASA-CR-160438) SHUTTLE ORBITER S-BAND
PAYLOAD COMMUNICATIONS EQUIPMENT DESIGN
EVALUATION Final Report (Axiomatic, Los
Angeles, Calif.) 181 p HC A09/MF A01

N80-15307

CSCL 17B G3/32

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SHUTTLE ORBITER S-BAND PAYLOAD COMMUNICATIONS EQUIPMENT
DESIGN EVALUATION

FINAL REPORT

Contract No. NAS 9-15792

(JSC Technical Monitor - William Seibert)

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Axiomatix Report No. R7911-4
November 30, 1979

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1.0 EXECUTIVE SUMMARY

1.1 Purpose and Scope

The overall objectives of the effort have been to critique the design and assess the performance of the Orbiter S-band communication equipment. The work has three principal aspects/goals:

(1) Review and analysis of the ability of the various S-band subsystem avionic equipment designs to interface with and operate on signals from/to adjoining equipment.

(2) Assessment of the performance of the hardware against the specified system and subsystem requirements.

(3) Critique of test plans, procedures and results of tests conducted on the S-band hardware LRU's.

TRW, Redondo Beach, California, is the hardware contractor for six S-band avionic systems or LRU's. These LRU's to which Axiomatix's efforts have been addressed are:

- (1) Network Transponder
- (2) Network Signal Processor (NSP)
- (3) FM Transmitter
- (4) FM Signal Processor (FMSP)
- (5) Payload Interrogator (PI)
- (6) Payload Signal Processor (PSP).

TRW's responsibilities include design, design analysis, breadboard, engineering model, flight unit production, and acceptance and qualification testing of each LRU. Although TRW has overall cognizance and builds most of the hardware, certain subassemblies are subcontracted to other manufacturers.

1.2 Approach and Execution

The general approach has been to work with cognizant NASA personnel and individuals at the principal prime contractor (Rockwell International) and equipment subcontractor (TRW). A vital part of the activity involved Axiomatix attendance and participation in the regular monthly program reviews, as well as all special meetings, at TRW and RI. At

these reviews, the status of each LRU was presented in a formal fashion. Technically detailed discussions, which did not necessarily require the attendance of all participants, were generally held at the end of the day or on the following day. These latter gatherings usually involved detailed discussions on design and specification issues that surfaced at the regular monthly reviews. Axiomatix also worked with TRW engineers on an ad hoc basis.

During the contract performance period, three preliminary design reviews (PDR's) were held and attended by Axiomatix. The PDR's covered the PSP LRU, PI LRU and the PI triplexer. Also, a number of special meetings involving Axiomatix engineers were held at TRW and RI. These gatherings addressed very specific issues and were instrumental in gaining consolidated understanding of various problems and, in most cases, pointed the way to solutions.

Axiomatix engineers spent extensive periods in review of design documents, critique of test procedures, and performing design verification analysis. Important results were communicated to appropriate NASA/JSC, RI and TRW engineers as soon as they were obtained. Each month, Axiomatix prepared a monthly technical report which contained a brief summary of all relevant technical activity, including design reviews, technical conferences, design and analysis efforts and results, critical problem areas, and a forecast of effort for the next monthly reporting period. Detailed results from evaluations or analyses of current interest were also appended to the monthly reports.

1.3 Summary of Activity, Studies, Results and Assessments

A major portion of the work over the contract period (approximately nine months) involved analysis and critique of the TRW-produced LRU's. Many of the issues addressed have been of concern for over two years. Since this report covers a limited time span, the reader who wishes to obtain a longer term historical perspective is referred to the previous equipment design report [1] which covered the period January 1978 through January 1979. (See, especially, Table 1 in the Executive Summary.) An issue outline covering the period February through October 1979 can be found in Table 3.1 of this report.

The following subsections present highlights, abstracted from the body of the report, on those subjects of primary interest. Numbers in parentheses following a statement refer to sections in which more detailed information may be found.

1.3.1 Payload Interrogator Evaluations

(1) The PI receiver input has been protected by a diode power limiter (in lieu of switched attenuator pads in the triplexer) which both protects the preamplifier from overload damage and allows the receiver to effectively function up to input power levels of +10 dBm (see subsections 3.2.2 and 4.1.2.2).

(2) Axiomatix was instrumental in convincing TRW that a non-coherent type AGC loop should be employed by the PI receiver for out-of-lock conditions and that the use of such an AGC would reduce the receiver false lock propensity (see subsections 3.2.3 and 4.1.5).

(3) TRW changed the technique of avoiding PI receiver side-band lock (false lock) from a dependence on lock detector threshold discrimination to preventing lock by use of a sufficiently rapid receiver sweep rate (see subsections 3.2.4 and 4.1.7).

(4) The current PI receiver design wideband output bandwidth is nominally 6 MHz rather than the specified 4.5 MHz--an unacceptable value for which some redesign will be necessary to correct (see subsections 3.2.5 and 4.1.3).

(5) The signal regulation loop of the PI wideband output to the various interfaces (PSP, CIU, KuSP) will be an RMS type located within the PI proper and will be responsible for some suboptimum link performance, especially as it affects the bent-pipe (see subsections 3.2.6 and 4.1.4).

1.3.2 Payload Signal Processor Evaluations

Axiomatix has reviewed the entire PSP design and has concluded that it is well-designed and embodies up-to-date implementations. Nowhere in the PSP circuits or performance measurements has Axiomatix found significant weaknesses nor are there any important open issues (see subsections 3.3 and 4.2.1).

1.3.3 Network Transponder Design and Performance

(1) The first and second IF modules are assessed as design and performance marginal (see subsection 3.4.1).

(2) The measured BER degradations which have been observed to occur in the STDN high-power duplex mode is apparently caused by some nonlinear action or ionic breakdown in certain RF connections fabricated from stainless steel and fitted with a Kovar center pin (see subsection 3.4.2).

1.3.4 FM Transmitter Performance

A problem with seemingly excessive frequency offset and drifts has been traced to the moisture content of the sealed units and is being remedied by more stringent vacuum bake procedures (see section 3.5).

1.3.5 Network Transponder Qualification Test Procedures

(1) The entire QTP for the network transponder was reviewed as to the nature of the tests, appropriateness of the tests, inconsistencies, omissions, usefulness of the test data, test procedures, equipment and methods, and was judged to adequately meet the intent of the test specification as a whole (see section 4.3).

(2) Some inconsistencies and omissions were discovered, and three items concerning thermal cycle tests, BER measurements and RF common port overload protection need some attention and resolution (see subsection 4.3.5).

1.3.6 ESTL Network Equipment Verification Tests Evaluation

(1) To date, only the ESTL STDN mode test procedures have been evaluated and, overall, these procedures are well thought out, well-written and generally meet the requirements as defined by "System Development Test Requirements and Status (TRAS) Report for STDN S-Band Direct Link," JSC 11300, September 28, 1977.

(2) Of the inconsistencies and omissions discussed, most have been addressed by the ESTL personnel. There is a major concern that some tests were conducted with the NSP in a mode which no longer reflects the current operational practices (see subsection 4.4.3.1).

1.4 Projections

(1) Future detailed involvement with respect to TRW's activity on the S-band network hardware LRU's will be oriented toward performance and malfunction problems.

(2) Design, circuit, and performance evaluation and supporting analysis will continue on the PI and PSP until they complete their critical design review and QTP phases.

(3) Review of the ESTL network equipment verification plans will be extended and completed with formal recommendations on problem areas.

2.0 INTRODUCTION

2.1 Statement of Work

2.1.1 Objectives

The overall objectives of the effort have been to critique the design and assess the performance of the Orbiter S-band communication equipment. The work has three principal aspects/goals:

(1) Review and analysis of the ability of the various S-band subsystem avionic equipment designs to interface with and operate on signals from/to adjoining equipment.

(2) Assessment of the performance of the hardware against the specified system and subsystem requirements.

(3) Critique of test plans, procedures and results of tests conducted on the S-band hardware LRU's.

The S-band hardware LRU's being produced by TRW to which the efforts have been addressed are:

- (1) Network Transponder
- (2) Network Signal Processor (NSP)
- (3) FM Transmitter
- (4) FM Signal Processor (FMSP)
- (5) Payload Interrogator (PI)
- (6) Payload Signal Processor (PSP).

2.1.2 Specific Tasks Outline

The contract statement of work specifies that the following principal tasks will be conducted over the contract period:

Task #1, S-Band Network Equipment Verification Plans Evaluation. Reviews the various verification test plans (especially by TRW qualification and JSC/ESTL system plans) as to appropriateness and validity, monitors tests and analyzes results.

Task #2, S-Band Payload Communications System Specification Review. Continually compares the equipment specifications (PI, PSP, KuSP, PDI, MDM/GPC) relative to the hardware design/performance to ensure that interface compatibility, performance requirements and operational needs are being met.

Task #3, S-Band Payload Communication Equipment Design Evaluation and Development Support. Performs detailed design and performance assessments of the TRW equipment designs, provides supporting analysis and experimental investigations of the functional circuits and recommends appropriate design changes to NASA, Rockwell and TRW.

2.1.3 General Approach

The general approach has been to work with cognizant NASA personnel and individuals at the principal prime contractor (Rockwell International) and equipment subcontractor (TRW). A vital part of the activity involved Axiomatix attendance and participation in the regular monthly program reviews, as well as all special meetings, at TRW and RI. These latter gatherings usually involved detailed discussions on design and specification issues that surfaced at the regular monthly reviews. Axiomatix also worked with TRW engineers on an ad hoc basis.

Each month, Axiomatix prepared a Monthly Technical Report which contained a brief summary of all relevant technical activity, including design reviews, technical conferences, design and analysis efforts and results, critical problem areas, and a forecast of effort for the next monthly reporting period. Detailed results from evaluations or analyses of current interest were also appended to the monthly reports.

Axiomatix engineers spent extensive periods in review of design documents, critique of test procedures, and performing design verification analysis. Important results were communicated to appropriate NASA/JSC, RI and TRW engineers as soon as they were obtained.

2.1.4 Correspondence with Related Activity

The work herein reported was related to and interacted with efforts performed under other active NASA contracts. Contract NAS 9-15240E and F, "Shuttle Ku-Band and S-Band Communications Implementation Study," involves the system aspects that tie together the S-band equipment in the performance of specific communication functions. Two other contracts, NAS 9-15409C, "Orbiter CIU/IUS Communications Hardware Evaluation," and NAS 9-15604C, "Shuttle/Payload Communications and Data System Interface Analysis," are concerned with the PI and PSP hardware from a functional payload communication link perspective. These latter studies are concerned primarily with interface and throughput issues.

2.2 Organization of the Final Report

The two sections following (4.0 and 5.0) address in detail the various aspects of the work performed.

Section 3.0 is an exposé of the ongoing issues and activities as they developed and were addressed at regular monthly reviews, PDR's and special technical meetings. Use has been made of tables and charts to summarize the vital nature of each important issue and to show its timeline history. Following this summary, selected topics are reviewed in greater depth.

In Section 4.0, supporting studies and analyses performed by Axiomatix are delineated. Since both the PI and PSP were subject to preliminary design reviews during the reporting period, each is given a comprehensive design and performance critique. Also examined in depth are the Network Transponder qualification test procedures (QTP's) and the ESTL network equipment verification plans.

2.3 Avionic Equipment and System Descriptions

Some readers may not be wholly familiar with the S-band hardware and the principal communication equipment with which it interfaces. As a primer, therefore, Appendix A contains a system overview followed by functional descriptions of the most important LRU's, including block diagrams.

As regards the PI and PSP, Appendix A does not include overview descriptions. Rather, detailed descriptions are found, respectively, in sections 4.1 and 4.2.1.

3.0 RESULTS OF MONTHLY REVIEWS, PDR'S AND TECHNICAL MEETINGS

TRW, Redondo Beach, California, is the hardware contractor for the six S-band avionic systems listed under section 2.1.1. TRW's responsibilities include design, design analysis, breadboard, engineering model, flight unit production, and acceptance and qualification testing of each LRU. Although TRW has overall cognizance and builds most of the hardware, certain subassemblies are subcontracted to other manufacturers.

As the means for regularly addressing all progress and problems, TRW scheduled monthly reviews which were attended by NASA, RI and Axiomatix personnel. (No review was held during the month of September 1979.) At these reviews, the status of each LRU was presented in a formal fashion. Technically detailed discussions, which did not necessarily require the attendance of all participants, were generally held at the end of the day or on the following day. Since the TRW monthly reviews were regularly attended by many readers of this report and handouts of the material presented by TRW were made available to each attendee, it is not necessary in this report to address all subjects and details. What is contained in the present report are summaries and assessments of those subjects/areas in which Axiomatix was intimately involved by virtue of the contract task statements.

During the contract performance period, three preliminary design reviews (PDR's) were held and attended by Axiomatix. A review of each is given in sections 3.2, 3.3 and 3.4, following.

Also, a number of special meetings involving Axiomatix engineers were held at TRW and RI. These gatherings addressed very specific issues and were instrumental in gaining consolidated understanding of various problems and, in most cases, pointed the way to solutions.

3.1 Summary of Important Issues/Problems and their Resolution/Status

Many of the subjects of concern are not new in that they have been at issue for periods of more than a year. Since this report covers about a nine-month time span, the reader who wishes to obtain a longer term historical perspective is referred to the previous equipment design report [1] which covered the period January 1978 through January 1979.

Table 3.1 summarizes the major issues. Issues prefixed with a + are ones of long standing and will be found addressed in [1]. If no issue prefix is indicated, the issue has surfaced within the last nine months.

Table 3.1. Major Issue Summary

	Issue	Issue Nature	Effort Toward Resolution	Resolution
3.2.1	PI Triplexer Design	Location of arc suppression diodes may cause EMI.	TRW examined configuration and believes that it will pass EMC testing.	Awaits EMC tests.
3.2.2+#	PI Receiver Input	<ol style="list-style-type: none"> 1. TRW desired a diode limiter in place of switched attenuators. 2. Receiver performance is undetermined for signal levels above -20 dBm. 	<ol style="list-style-type: none"> 1. TRW obtained limiter and conducted tests to show that it would work without compromising performance. 2. TRW conducted tests up to +10 dBm signal levels. 	<ol style="list-style-type: none"> 1. Limiter replaced attenuator pads in the triplexer design. 2. Receiver performed within specification for levels up to +10 dBm.
3.2.3*	PI Receiver Preacquisition AGC	Receiver has no AGC prior to lock when coherent AGC is obtained.	Axiomatix recommended the use of a noncoherent AGC. TRW studied the performance and chose to adopt the noncoherent AGC approach.	Noncoherent AGC is now employed when the receiver is out of lock.
3.2.4+#	PI Receiver False Lock Susceptibility	<ol style="list-style-type: none"> 1. The receiver should not lock onto carrier sidebands that are ≤ -26 dBc. 2. Receiver false lock performance is undefined for nonstandard payload modulations. 	<ol style="list-style-type: none"> 1. Lock detector threshold discrimination was initial solution. This has been supplanted by a critically fast sweep rate method. 2. Axiomatix defined allowable modulation forms and parameter ranges. 	<ol style="list-style-type: none"> 1. Testing shows that the requirement will be met by the fast sweep rate. Some performance questions remain. 2. A revised payload ICD will incorporate the Axiomatix-generated constraints.

Table 3.1. Major Issue Summary (Cont'd)

Issue	Issue Nature	Effort Toward Resolution	Resolution
3.2.5# PI Receiver Wideband Output Bandwidth	The 3 dB bandwidth is specified at 4.5 MHz. The PDR disclosed it may range between 4.5 & 8 MHz, depending upon conditions. A wide bandwidth may compromise Ku-band link performance.	TRW is to investigate alternative filter specifications and IF and baseband circuit designs to correct the problem.	Open issue.
3.2.6+ PI Receiver Wideband Output Regulation	<ol style="list-style-type: none"> 1. Incompatibility between PI and KuSP specifications. 2. An RMS type regulator does not optimize bent-pipe link performance. 3. The regulator should be in the KuSP in order to handle attached payload inputs. 	<ol style="list-style-type: none"> 1. A working committee was established to define the interface specification. 2. An RMS regulator was selected rather than a peak regulator due to high redesign costs. 3. Costs of placing the regulator in the KuSP were unacceptably large. 	<ol style="list-style-type: none"> 1. Compatibility established. 2. Suboptimum bent-pipe performance for certain types of waveforms will be tolerated. 3. Regulator will remain a part of the PI and attached payload inputs to the KuSP will not be regulated.
3.2.7+# PI Receiver Sweep Range	The initial design sweep was too small to cover the worst-case frequency error & PI transmitter sweep turn-around frequency limits.	Analysis by both Axiomatix & TRW defined the proper sweep range maximum values. Requirement must be regularly updated.	Sweep range design as of the PDR is probably OK, but marginal.

Table 3.1. Major Issue Summary (Cont'd)

Issue	Issue Nature	Effort Toward Resolution	Resolution
3.2.8# PI Receiver Tracking Loop Phase Error	<ol style="list-style-type: none"> 1. Maximum static phase error is specified at 3°. The receiver SPE compatibility is about 8°. 2. TRW has included the circuit phase error between the tracking loop and wideband phase detector in the SPE accounting. 	<ol style="list-style-type: none"> 1. Axiomatix believes the 3° specification is too strict; 8° due to biases is acceptable. 2. Axiomatix recommended that the subject error not be included in the SPE accounting in terms of meeting the Rockwell specification. 	<ol style="list-style-type: none"> 1. Specification revision recommended. 2. TRW accepted the recommendation.
3.2.9+ PI Transmitter Phase Noise	The phase noise performance remains unknown and analytical predictions are not assuring.	Axiomatix has requested that TRW measure the spectrum on the breadboard synthesizer and transmitter. Axiomatix will evaluate results.	Open Issue.
3.2.10 PI Transmitter Sweep Rate	The two sweep rates of 30 kHz/s and 540 Hz/s are generally improper for most anticipated payloads.	Analysis by Axiomatix as to proper rates & review of circuit performance capabilities by TRW have lead to a lowering of the rates.	The nominal sweep rates have been reduced to 10 kHz/s and 250 Hz/s.
3.3.1 PSP Command Idle Pattern	The Rockwell specification called for the pattern to begin with a "1", but no end state specification was given.	Axiomatix requested that possible requirements for a specified end state be investigated.	The specification has been amended to call for the idle pattern to end with a "0".

Table 3.1. Major Issue Summary (Cont'd)

	Issue	Issue Nature	Effort Toward Resolution	Resolution
3.3.2+	PSP Performance Losses	Overall PSP degradation is specified at -1.5 dB. Partitioning of the loss between the subcarrier tracking loop and bit synchronizer is unknown.	Breadboard-measured maximum losses for both the tracking loop and synchronizer working together are about -0.8 dB.	Partitioning of the loss has been determined unimportant since the combined loss is so far below the maximum limit.
3.4.1+	Network Transponder First and Second IF Modules Critical Performance	The first and second IF modules have a history of marginal performance and have been very difficult to align to maximum performance specifications.	Through critical parts screening and selection plus very strict alignment procedures and testing, the problems have been minimized and no redesign has been necessary.	Issue closed.
3.4.2	Network Transponder BER Degradation in the Duplex Mode	Measurements at TRW, AIL and ESTL have all disclosed that significant and unexplained losses, as measured by observed BER, occur in the duplex operating mode.	A series of tests over a nine-month period have isolated the majority of the problem to some peculiarities of the preamp assembly RF connectors.	Final resolution not made. A likely solution is replacement of the connectors with ones which do not have the manifest problem.
3.5+	FM Transmitter Frequency Drift	Most units have shown a general and significant upward frequency drift over a long period of time. Some shift in units having accumulated shelf (off) time has also been observed.	Design analysis and tests have shown that accumulated moisture may affect the units and, in particular, a certain capacitor in the frequency-determining circuits.	Problem not completely resolved but some production changes with regard to increased subassembly and LRU vacuum bake time to remove residual moisture has apparently brought the problem under control.

Where a # is used, the problem arose due to the PI PDR in October. And, where +# occurs, the issue is old, was once supposedly resolved but has been reopened by the PI PDR. Each of the issues is addressed in discussion form under the appropriate section headings following.

Finally, Figure 3.1 portrays the issues on a calendar basis, indicating their beginnings, periods of activity when Axiomatix made active contributions and point of resolution (or probable resolution). Figure 3.1 includes past history/progress/resolutions from the standpoints that it repeats the CY78 activity as taken from Figure 7, page 30, of [1]. Note that a number of issues have been opened and closed two or more times.

3.2 Payload Interrogator Issue Discussion

3.2.1 PI Triplexer Design

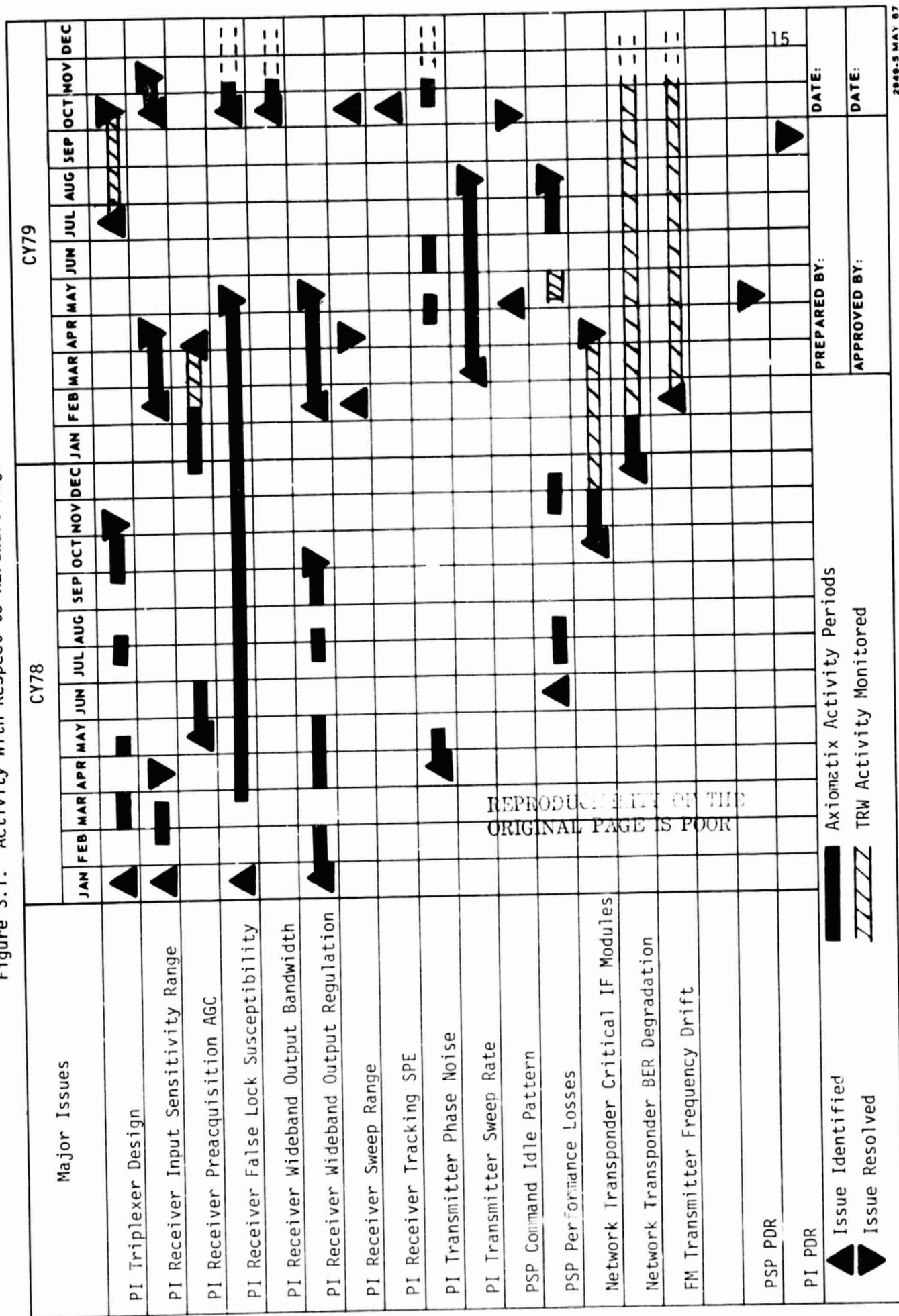
Transco, the triplexer supplier, elected to mount the arc suppression diodes for the coaxial switch coils external to the switch housings as a method of ensuring switch reliability. (The logic of this approach has not been fully comprehended.) A question therefore arose as to if, because the diodes and their leads are unshielded, an EMI problem is created. It was noted that, by definition, the switches are pulsed only during nonoperational (i.e., nonreceiving) periods. Although this may be correct and any EMI (it is only momentary in nature) created by the switches should not affect the PI operation, it could have an effect on other avionics equipment.

Analysis and some measurements made by Transco show that EMI should not be a problem. TRW is confident that the configuration will pass EMC tests when the triplexer is fully enclosed within the PI housing.

3.2.2 PI Receiver Input Sensitivity Range

At the February 1979 TRW monthly program review, a problem was outlined concerning excessive size of the sensitivity attenuator pad transfer switches within the triplexer (see section 5.1 of [1] for a description). One proposed solution was to replace the two transfer switches with four SPDT coax switches which could be fitted into the triplexer physical envelope. A second solution, and the one most favored by TRW, was to eliminate the attenuators and switches completely, replacing them with a breakdown diode power overload protector for the preamplifier input.

Figure 3.1. Activity With Respect to Hardware Major Issues



This solution assumes that the only purpose for the baseline attenuators is that of protecting the preamplifier from overload and possible burnout conditions.

One objection raised to the breakdown diode power limiter was that it could possibly introduce in-band spurs into the receiver for high signal levels as a result of the nonlinear diode characteristics. TRW was therefore requested to obtain and test the limiter for intermodulation products for several interference signal conditions. The results of these tests, presented at the March monthly review, proved negative. Furthermore, the diode limiter characteristic showed that the maximum output of the limiter was +13 dBm for an input signal level of +22 dBm and less than 13 dBm for all other input levels up to 1 W (+30 dBm). Since the preamplifier maximum allowable input is +20 dBm, a 7 dB protection margin is obtained with the limiter.

Axiomatix believed that the diode limiter would serve to protect the preamplifier and that it would not generate significant in-band spurs. There was, however, a question of receiver signal level back-off and if such capability should be retained. The question was not one of impropriety of the limiter but if the entire PI receiver could function properly under a condition of front-end limiting in the preamplifier, first mixer and first IF circuits--a condition that the input power protector cannot obviate. Thus, if the baseline design selectable attenuator pads were deleted from the triplexer (in favor of using the input power overload protector exclusively), there would be no way of backing off the input power to a point where receiver limiting is prevented (input signal level < -20 dBm).

A decision was made by TRW and RI to proceed with incorporation of the diode limiter and to eliminate all switchable pads. No tests, however, were subsequently conducted to determine if the receiver would function properly above -20 dBm. Axiomatix therefore submitted a RID at the October PI PDR requesting TRW to conduct the necessary tests and determine to what limit above the -20 dBm level the receiver can be expected to provide nondegraded output and remain essentially immune to false lock. TRW quickly responded and provided the information tabulated in Table 3.2 which shows that, at an RF carrier level of +10 dBm (a level at which the IF stage amplifiers are saturated), the receiver performs essentially the same from a false lock perspective as it does at -20 dBm. Output waveform degradation measurements have not yet been made.

Table 3.2. PI Receiver Strong Signal False Lock Performance

RF Frequency	RF Input Level	Sideband False Lock Level
2209.926 MHz	+10 dBm	-27 dBc
	-20 dBm	-26 dBc
	-50 dBm	-26 dBc
2210.074 MHz	+10 dBm	-26 dBc
	-20 dBm	-26 dBc
	-50 dBm	-25 dBc

3.2.3 PI Receiver Preacquisition AGC

Axiomatix determined more than one year ago that the lack of receiver gain control during periods when the coherent tracking loop was out of lock and, therefore, coherent AGC is not generated, was giving rise to several problems--false lock states, in particular. (See section 6.1.1, page 133, of [1] for the detailed assessment.) Our recommendation to TRW in January 1979 was that a noncoherent AGC voltage should be generated when the receiver is out of lock and used to set the overall receiver gain. After showing TRW the expected performance, they readily adopted the suggestion and redesigned the AGC portions of the receiver. Breadboard tests have proven that excellent performance is obtained. Additional details on the design of the receiver AGC subsystem may be found in section 4.1.5.

3.2.4 PI Receiver False Lock Susceptibility

The problem of avoiding lock on small discrete frequency type sidebands that fall within the PI receiver acquisition frequency sweep range has been considered in great depth. Sideband lock has been given the generic designation "false lock." Extensive analysis on the subject appears in [1], Section 5.3, pp. 66-89, and in [2], Section 5.1, pp. 65-89.

Prior to new information supplied by TRW at the October PI PDR, the capability of the PI receiver to preclude false lock was based upon the operation of the PLL lock detector and its discrimination against inhibiting receiver sweep frequency acquisition with respect to small discrete

sideband levels as compared to that of the true carrier component. Axiomatix had identified several basic and mechanistic problems with the TRW approach, as follows:

- (1) The "threshold" of false lock (generally specified by TRW to be -26 dBc) would have a large tolerance due to AGC and lock detector bias errors.
- (2) There was a range of uncertainty below -26 dBc over which false lock may or may not occur, depending upon various conditions.
- (3) The lock detector filter bandwidth was sufficiently wide to pass the true carrier beat note frequency with enough amplitude that the receiver sweep could be discontinued prematurely.
- (4) Overall performance was basically not analyzable and would have to be determined by measurements.

It was revealed at the recent PI PDR that the basic philosophy or mechanism by which the PI receiver is rendered immune to sidebands lock has been changed. The new approach has been given a preliminary evaluation by Axiomatix and determined that it may be classified as a False Lock Avoidance (FLA)* technique rather than the False Lock Detection (FLD)* method which characterized the earlier design. It is believed that the change is good in that it results in somewhat better understood and more predictable performance. The method involves sweeping the receiver VCO sufficiently fast that sideband lock is precluded. This approach was suggested by Axiomatix a year ago, but was not considered practical because of the nearly complete design state of the receiver at that time. Subsequent problems with the receiver breadboard operation, however, forced TRW to adopt the faster sweep (approximately 330 kHz/s rather than 10 kHz/s).

Since the change is so recent, full evaluation has not been made. The basic theory and circuit mechanisms are discussed under section 4.1.6.

3.2.5 PI Receiver Wideband Output Bandwidth

At the PI PDR, it was disclosed that the receiver wideband output bandwidth could be expected to range between 4.5 MHz (specification value) and 8 MHz as a function of received signal operating level and filter element

* See [1], pp. 66-67.

tolerances. A RID was initiated by Axiomatix on this issue. Axiomatix believes that a bandwidth on the order of 8 MHz could compromise Ku-band link performance. Axiomatix also maintains that noise bandwidth rather than 3 dB bandwidth should be the critical measure of output bandwidth.

The wideband output lowpass bandwidth of the current receiver design is not established solely by the lowpass filters following the wideband phase detector (as had previously been believed based upon conceptual design information). Rather, the last IF filter just prior to the wideband phase detector is the most influential in meeting the 4.5 MHz lowpass requirement. This filter has a 3 dB bandwidth of about 12 MHz (6 MHz lowpass equivalent) while the actual lowpass filters in the base-band circuits have respective bandwidths of 12 and 8 MHz. TRW's design philosophy has been to base the overall bandwidth on the cascade of the bandpass and lowpass filters in a manner wherein all these filters have a significant contributing effect. The result is that, with temperature and signal operating level variation (AGC) effects, plus allowances for component tolerances, the effective 3 dB lowpass bandwidth may range anywhere between 4.5 and 8 MHz. Thus, 4.5 MHz is the low-end limit; the expected bandwidth is on the order of 6 MHz.

In their analysis supplied to date, TRW has even included the triplexer ripple characteristics in their result. Although this may be appropriate to signal transfer, it has no effect on the noise produced at receiver output as the effective noise sources follow the triplexer. It is Axiomatix's position that noise bandwidth is more important than signal bandwidth. To this end, therefore, TRW is in the process of reviewing their design with an eye to widening the IF bandwidth and narrowing the output LPF bandwidth.

As this report is being written, TRW is in the process of several activities to determine how the problem may be circumvented without the need for major redesign. Their investigation will include:

- (1) Measurement of the output noise equivalent bandwidth on the receiver breadboard
- (2) Analysis of decreasing the bandwidth of the post-detection (output) lowpass filter.

(3) Review of IF bandwidth filter requirements.

Axiomatix will follow this activity closely. In addition, Axiomatix will perform an independent assessment, the beginnings of which are summarized in section 4.1.3.

3.2.6 PI Receiver Wideband Output Regulation

The issue of what type of regulator is needed and where it should be located (PI versus KuSP) has a long-term history which may be summarized as follows.

Axiomatix had previously analyzed the required nature of the output signal regulator in order to optimize the performance of the bent-pipe link. (See [1], subsection 4.2.1.1, pp. 31-36, and [2], subsection 4.3.2, pp. 57-59, subsection 4.4.2, pp. 63-64, and section 5.4, pp 134-149.) A signal-peak type of regulating loop located in the KuSP, rather than an RMS type of loop within the PI, was Axiomatix's recommended approach.

Hughes Aircraft (the KuSP hardware subcontractor) was requested to provide engineering and cost estimates for including the peak regulator in the KuSP. This information was made available at the February Hughes monthly review but was judged by NASA and RI to be too costly. As a result, TRW was asked to estimate the cost of redesigning the baseline PI RMS regulator so that it would have a peak regulating capability. TRW's estimates also proved to be quite costly. The final approach, therefore, was to retain the RMS regulator and accept the overall suboptimum performance of the wideband bent-pipe link.

Having made this decision, the final problem was to properly define the signal interface between the PI and the units to which the wideband output interfaced, namely, the PSP, KuSP and CIU (payload station). Again, Axiomatix presented the results of analysis involving the peak-to-peak to RMS ratios for various types of expected output waveforms. It was decided that some noise peak clipping (and the resultant loss in SNR) could be tolerated for the KuSP interface (bent-pipe link), but that a lesser amount of clipping should be allowed at the inputs of the PSP and CIU. Finally, it was resolved at a meeting held at RI on April 26, 1979 that the specification of the PI wideband outputs should be the following:

Output to PSP and CIU

2.0 \pm 0.4 V RMS
8 V p-p maximum

Output to KuSP

2.0 \pm 0.4 V RMS
7 V p-p maximum

This resolution was based in part on the fact that the TRW regulator characteristic is, in fact, reasonably close to a true RMS measure ($\sqrt{2}$) as determined by breadboard measurements.

For details concerning the RMS regulator and output circuits design and performance, see section 4.1.4.

3.2.7 PI Receiver Sweep Range

The frequency range over which the PI receiver must sweep to search for carrier lock due to nominal frequency uncertainty has steadily widened over the past year. Originally specified at ± 50 kHz, the range grew to ± 70 kHz (Amendment C-01) and then became ± 85 kHz early in 1979 (Amendment C-01, Revision C). These increases were due primarily to the underlying frequency stabilities associated with the independent frequency sources employed in the PI transmitter and receiver, and viewed worst-case when the two subsystems operate as a pair. In February 1979, Axiomatix reviewed the then understood design and performance status and predicted that the range could be as large as ± 145 kHz. At the October PI PDR, TRW presented that the minimum requirement was then ± 111 kHz and that worst-case (due to temperature variation, production tolerances and aging) may be ± 132 kHz. The measured breadboard receiver performance shows a minimum range of ± 111 kHz and a maximum range of ± 121 kHz over temperature. Thus the situation would appear to be somewhat marginal.

Little additional information is available from TRW. Their PDR Data Package, Volume I, page 4-27, indicates, after some redesign to incorporate a 300 kHz narrow IF filter (rather than 200 kHz), that the nominal sweep range will be ± 125 kHz. Minimum capability can be expected as ± 111 kHz, and maximum range could be ± 132 kHz. Presently, it is somewhat confusing as to whether a problem does or will exist.

3.2.8 PI Receiver Tracking Loop Phase Error

TRW estimates that up to 8° of equivalent tracking static phase error (SPE) may accrue due to uncontrollable direct voltage offsets in the PLL circuits. The total specification on PLL SPE is 3° . It should be noted

that the 3° is allowable for static frequency error. Since the DC loop gain for TRW's design is very large, frequency offset SPE is no problem. Axiomatix feels that the specification is somewhat strict and perhaps not appropriate in light of TRW's approach but, before a new value is suggested, a better understanding of the receiver's true capability is needed.

TRW has identified a second type of phase error, namely, that which will exist between the PLL phase detector reference and the wideband detector reference (due to uncompensated circuit phase shift.) A 6° value has been advanced for this phase error by TRW; Axiomatix believes that this is a reasonable value. The number has not been specifically specified by RI. TRW should not, however, add the 6° figure to the 8° and indicate that the maximum static phase error is out of specification by 11° .

Further identified by TRW is a dynamic (but constant) phase error due to the need to track the frequency ramp generated by sweeping the PI transmitter and "turned around" by the payload transponder. The value is 1.7° . No detailed analysis supporting this number appears in the PDR documentation. Since, for an imperfect second-order PLL, this dynamic phase error increases with time, additional investigation of this area is warranted. The maximum mean tracking phase error for all sources combined is not to exceed 15° . Clarification of definition appears to be needed.

3.2.9 PI Transmitter Phase Noise

The early issue on transmitter phase noise centered on if the integrated phase noise from the carrier frequency plus 10 Hz to some arbitrarily large relative value (say, 5 MHz) would be less than 10° RMS. DS payloads having transponder receiver bandwidths as small as 13 Hz (at absolute threshold) formed the basis for the specification. Subsequent studies, however, determined that, at maximum Orbiter/payload communication distances, the minimum expected operational DS transponder receiver bandwidth shouldn't be less than 150 Hz. This, in turn, suggests that some relaxation of the specification may be in order. But, before any such determination can be assessed, adequate measurements of the PI transmitter phase noise spectrum must be made. Analyses performed by TRW to date are not assuring without experimental verification. Axiomatix has therefore submitted a RID to request that TRW measure the phase noise spectrum from the carrier frequency plus 10 Hz to the carrier frequency plus 5 MHz. Axiomatix will evaluate the potential phase noise magnitude and implications once the spectrum measurements become available.

3.2.10 PI Transmitter Sweep Rate

It had been established from information supplied by JPL concerning the frequency ramp tracking rate of the DS standard transponder that the maximum tolerance 600 Hz/second PI transmitter sweep rate would likely be too rapid for reliable transponder receiver acquisition.

At a meeting held at RI on April 26, 1979 to review PI specification issues and problems, the question of an appropriate PI transmitter slow sweep rate for DS payloads was again raised. Suggestions were made to the effect that perhaps the sweep rate should be lowered to 100 Hz/second (rather than the 540 ± 60 Hz/s). TRW commented that their design approach of using an RC-type of integrator to provide the sweep voltage triangular waveform could not be easily changed to provide the lower rate without some sacrifice in linearity. Since linearity was considered to be a "soft" requirement, TRW was requested to perform some evaluation tests on the breadboard transmitter to ascertain just how low the sweep rate might be reduced without the need for major redesign. TRW conducted tests on the PI transmitter breadboard which showed that the $540 \text{ Hz} \pm 10\%$ sweep rate could be lowered to $100 \text{ Hz} \pm 40\%$ without changing the basic circuit design or construction. Of the $\pm 40\%$ tolerance, $\pm 23\%$ is sweep period variation and the remainder is attributed to variations from a straight line.

One problem with a 100 Hz/second rate is the very long time necessary to sweep the entire frequency uncertainty range of ± 33 kHz. It would take 11 minutes since the sweep profile is such that the total range must be covered twice. Axiomatix therefore felt that, although the sweep rate certainly ought to be lowered, 100 Hz/second could be unnecessarily too slow. For this reason, Axiomatix undertook an analytical study to determine the proper sweep rate for the minimum operating conditions that would prevail between the Orbiter and DS payload.

Axiomatix's analysis involved the use of the phase-plane method to obtain critical sweep rate values as a function of PLL natural frequency and damping factor. Of particular importance is the fact that over the conditions of interest, the DS transponder has a damping factor on the order of 3. After obtaining by computer solution the critical or absolute maximum values, a 20% backoff criterion was applied to allow for mechanistic performance. In addition, the sweep rate specification was based upon the transponder tolerance minimums in order to guarantee that the sweep rate would be proper for any transponder.

It was finally established through working with TRW engineers that a $\pm 30\%$ tolerance on the sweep rate would be appropriate. Thus, the new specified rate was selected so that the $+30\%$ value would equal the 20% absolute maximum backoff from the value calculated for the least favorable transponder tolerance conditions.

The new slow sweep rate for the PI transmitter is 250 Hz/second $\pm 30\%$. This value has been incorporated into the TRW design and appears in Rockwell's Revision B-C02 amendment.

3.3 Payload Signal Processor Issue Discussion

3.3.1 PSP Command Idle Pattern

At the PSP PDR, Axiomatix submitted a RID against the command idle pattern specification which, at that time, read:

"The idle pattern of alternating '1's and '0's starts with a '1'."

Axiomatix suggested that, if the idle pattern start state is specified, perhaps the end state should also be specified. The result has been a specification change, to wit:

"The idle pattern of alternating '1's and '0's starts with a '1' and ends with a '0'."

3.3.2 PSP Performance Losses

In [1], pages 34, 48 and 140, Axiomatix expressed concern over PSP internal losses due to subcarrier tracking error, bit synchronization errors and implementation-related degradations. Much of this early concern was due to insufficient design and performance details from TRW. These problems have more recently been dispelled by various actions.

The PSP PDR supplied answers to essentially all of the questions and, as a result of the details and data supplied, all major concerns were resolved. In particular, the SNR degradation performance of the combined subcarrier and bit synchronizer tracking loops was determined by breadboard measurement to be -0.8 dB for worst-case conditions. Since the specified overall loss is not to exceed 1.5 dB, there is sufficient margin, and it is relatively unimportant as to the partitioning of loss between the two loops. Diagnosis with an eye to improvement is not needed.

3.3.3 Minor Specification Changes Identified by the PSP PDR

The PSP PDR was held at TRW on May 2-3, 1979. The review was well prepared and presented, and no significant problems in design were uncovered. TRW has done an outstanding job of designing the PSP in a technically excellent fashion to comply with the design and performance specifications. Axiomatix's detailed assessment of the PSP design and performance is presented under section 4.2.

Four over-specification items were noted by TRW, as follows:

- | | |
|---|---|
| (1) Power | 32W versus 26W |
| (2) Initialization Time
Upon Power Transient | 3 ms versus 1 ms |
| (3) Initial Command
Data Output Time | 1.5 bit time versus 1.0 bit time |
| (4) Input Common Mode
Rejection | ≤ 40 dB (0-1 MHz) and < 30 dB (1-2 MHz)
versus ≤ 40 dB (0-2 MHz) |

No objections were raised concerning these items and RI took an action to incorporate them into a specification amendment.

As of the writing of this report, the PSP design is complete. Four recent PSP/MDM interface changes are in the process of implementation. These changes resulted from RID's submitted at the May 2-3 PSP PDR. In terms of the EM breadboard which is essentially complete through the assembly phase, the changes will be effected by means of "haywires" on the command processor boards.

3.4 Network Transponder

3.4.1 IF Module Critical Performance

As reported on page 141 of [1], the network transponder second IF module has had a chronic problem in terms of alignment and maintaining performance specifications with time. More recently, the first IF modules in the flight LRU's were found to exhibit degrading "dips" in their frequency response and had to be realigned. It was determined that the procedures employed upon initial adjustment were not correct.

These modules have been assessed as marginal by Axiomatix due to the basic nature of their analog circuit design. TRW has solved the most pressing problems--not by redesign--but by critical parts screening and selection, and exhaustive alignment and performance verification on the part of the original design engineer. Although this approach has proven effective in the short term, the long-term performance/reliability would appear to be speculative, and it is wondered how effective future "repairs" will be if wholly different individuals are involved.

3.4.2 BER Degradation in the Duplex Mode

Early in 1979, ESTL tests of bit error rate (BER) utilizing the network transponder in the STDN high-power duplex mode showed a marked performance decrease relative to that of nonduplex or power amplifier off operation. ESTL had measured losses in excess of 1 dB while TRW had independently (using different equipment) noted losses on the order of 0.5 dB. The following summarizes the chronology highlights of the investigations that followed.

Initially, diagnostic tests by TRW of the observed STDN high-power duplex mode BER degradation began to narrow the probable cause to receiver increased noise figure due to suspected leakage in the diplexer. TRW consistently measured an NF increase of 0.4 dB, which correlates well with the observed BER degradation of 0.5-0.6 dB. The problem did not appear to be caused by spurs or frequency coherence conditions.

As the testing continued, it rapidly became apparent that there was no readily identifiable cause for the problem but, rather, it appeared to be some elusive "gremlin" within the transponder. Thus, in order to isolate the source, a series of tests involving equipment substitutions and configuration changes took place. The results of this activity may be summed up by the following observations (expressed by TRW after about four months of testing):

(1) NF degradation is the same with the power LRU amplifier and the AIL TWT amplifier

(2) BER degradation is approximately 0.2 dB higher than NF degradation, probably due to test set contributions for BER

(3) BER degradation is approximately the same for the AIL test diplexer and the NASA triplexer

(4) BER is approximately the same for the AIL paramp and the Avantek transistor amplifier

(5) BER degradation is subject to variations which appear to be related to phasing and temperature

(6) The most significant contributor to high values of BER degradation appears to be the diplexer:

(a) Previous test results indicate BER degradation is primarily caused by the preamp LRU

(b) BER degradation does not change when the paramp is replaced with a transistor amplifier

(c) High BER degradation in the qualification preamp LRU is definitely caused by the diplexer and/or connectors.

As time increased, the possibility grew that the diplexer/preamp connectors were the source of the problem. Some tests were conducted to determine if the hermetically sealed connectors used within the diplexer/preamplifier assembly were operating nonlinearly as a function of incident power. Since the cables and their connectors within the assembly could not be changed, some special cables with hermetically sealed connectors were fabricated and added in series with the cable from the test set to the preamplifier. The theory was that, if the connectors were a problem, addition of the external cable with its connectors would result in further degradation. In order to negate the effects of the added cable apart from the hermetically sealed connectors, tests were also run with "identical" cables having commercial connectors. The tests appeared to indicate that, indeed, the additional hermetically sealed connectors contributed about 0.2 dB of degradation as measured by BER. However, Axiomatix cautioned that the test results should be regarded as inconclusive (at that stage) because:

(1) The performance degradation observed was within the accuracy tolerances of such tests

(2) No attempt was made to determine if the hermetically sealed connector cables and the commercial connector cables were truly "identical" in terms of insertion loss, VSWR, etc.

(3) The tests were based upon only one cable tested for the stated condition only.

Continuing tests disclosed no additional possible reasons for the BER losses. The evidence continued to show that the most probable causes were a combination of VSWR and RF connector heating which might invoke some sort of contact metal "diode phenomena." During September, AIL and NASA conducted some rather conclusive tests which verified that some phenomena associated with the connectors does cause the BER degradation. Two significant observations were made:

(1) Replacement of the qualification unit J2 connector (a connector with magnetic stainless steel shell and Kovar center pin) with a commercial (brass) connector reduced the test case noise figure degradation from 0.7 to 0.1 dB.

(2) Application of a magnetic field perpendicular to the normal J2 connector using Alnico magnets reduced the test case noise figure degradation from 0.7 to 0.1 dB.

The mechanism by which the magnets reduce the degradation is essentially unknown; it is suspected that the magnetic field effectively saturates the connector shell and Kovar pin so that the nonlinear action resulting in the degradation is suppressed.

ESTL also conducted a series of tests in both the STDN and TDRS transponder operating modes for which a magnetic field was applied to the J2 connector. The results of these tests are summarized as follows:

(1) Degradation with power amplifier on varies between 0.7 and 1.6 dB

(2) Degradation is not affected by TDRS spreading, convolutional encoding or encryption/decryption.

(3) Use of magnets with 1000 gauss strength caused degradation reductions of 0.5-0.8 dB in the high-frequency mode and 0.1-0.3 dB in the low-frequency mode.

A recent analysis made by TRW shows that the transmitter dummy antenna high-power load temperature rise can contribute up to 0.3 dB of noise figure increase.

Finally, some tests at both AIL and TRW indicate that there may be some intermittent ionic breakdown in some of the cables under high-power stress. Further effort is needed to verify this possible problem.

Just what the final resolution will be is not yet fully apparent. Based on all the evidence to date, the plan would appear to call for replacement of all J2 connectors exhibiting the above-mentioned degradation phenomena with approved equivalents having nonmagnetic properties.

3.5 FM Transmitter Frequency Drift

It was noted in [1], page 51, that two FM transmitters had experienced an unexplained upward frequency drift over a protracted period of time. Figure 3.2 graphically portrays the history of S/N 202. Initial investigations disclosed that the problem was not caused by run-away in the temperature compensation circuits associated with the frequency oscillator.

All evidence to date indicates that the real problem is probably the effects of moisture on several of the frequency-determining capacitors that are not hermetically sealed. Moisture tests on an Erie capacitor showed that it was capable of a 0.18 pf change for a 0-96% humidity change. This, in turn, could result in a 700 kHz frequency variation.

Two production changes resulted from the months of investigation into the FM transmitter drift problem, as follows:

- (1) Increase subassembly vacuum bake from 12 to 24 hours and implement environmental control subsequent to bake
- (2) Add a 24-hour LRU vacuum bake with cover removed just prior to sealing.

In addition, the ESTL LRU will have its Erie capacitor (suspected to have a high moisture sensitivity) changed for a sealed capacitor and the unit will then continue to be monitored to ascertain its drift history.

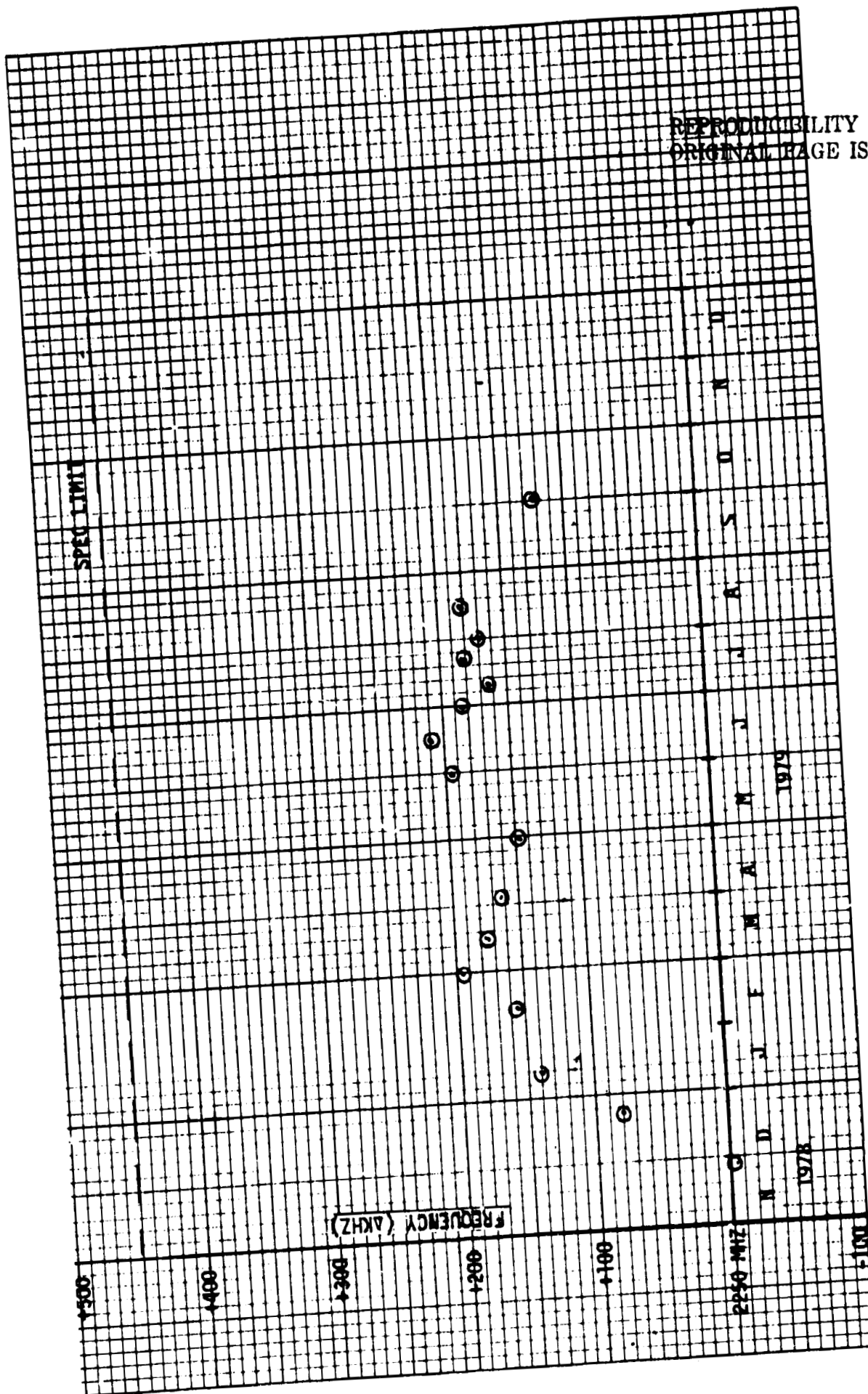


Figure 3.2. Frequency Drift History for FM Transmitter S/N 202

4.0 AXIOMATIX SUPPORTING STUDIES AND ANALYSES

4.1 Assessment of the PI Design and Performance

A preliminary design review on the Payload Interrogator (PI) was held by TRW October 10-11, 1979. As a result of this PDR, a large data package (D02694) covering the PI design, performance analysis and test data was made available.

In the following subsections, Axiomatix presents its evaluation of the PI design. Several objectives are considered, including:

- (1) Design soundness
- (2) Circuit integrity
- (3) Alternative approaches (that may have been better)
- (4) Performance critique
- (5) Expected future problems.

The subsection topics or headings are representative of the areas that have received the most attention by Axiomatix over the two-year period in which the PI design has evolved.

4.1.1 Overall Philosophy

Basically, the PI is a transceiver consisting of a receiver and a transmitter which are frequency excited or referenced to a universal frequency synthesizer that allows the PI to operate on any of 861 channel pairs. The transmitter operates on two distinct bands--1763-1840 MHz (L-band) and 2025-2120 MHz (S-band) and the receiver covers the band 2200-2300 MHz (S-band). Table 4.1 lists the principal operating characteristics of the receiver, and Table 4.2 are those for the transmitter.

Figure 4.1 shows a functional block diagram for the PI and will be used to illustrate the following descriptive discussion.

A single RF port connects the PI to the payload antenna cable as the payload antenna serves to simultaneously receive and transmit signals. This port connects into the receiver input and transmitter output through an assembly known as the triplexer. The triplexer consists of six cavity-based bandpass filters which divide the receiver band and both transmit bands approximately in half. A detailed description of the triplexer is found under section 4.1.2. Immediately following the triplexer receive switch and located at the input to the preamplifier is a power overload

Table 4.1. Principal PI Receiver Characteristics

Parameter	Value	Units
Input Frequency Range	2200 - 2300	MHz
Input Signal Level Operating Range	-124 to +10	dBm
AGC Range	-124 to -20	dBm
Noise Figure	7.0 max	dB
Thresholds: Acquisition	-122.5	dBm
Tracking	-124.0	dBm
Acquisition Sweep Range	± 125	kHz
Acquisition Sweep Rate	330	kHz/sec
Frequency Rate Tracking	17	kHz/sec
False Lock Immunity	Sidebands < -26	dBc
Tracking Bandwidth	3200	Hz
Maximum Phase Noise	15	Degrees-RMS
Maximum SPE	10	Degrees
Throughput Bandwidth	< 5.5	MHz
Output Signal Regulation	2.0 ± 0.4	VRMS
Throughput SNR Losses	2.1 max	dB

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Table 4.2. Principal PI Transmitter Characteristics

Parameter	Value	Units
L-Band Frequency Range	1763 - 1840	MHz
S-Band Frequency Range	2025 - 2120	MHz
Carrier Frequency Tolerance	± 0.0012	%
Carrier Phase Noise	10 max	degrees-RMS
Output Spurs	< -65	dBc
Phase Modulator	0.2 to 2.5	radians
Frequency Sweep Ranges	± 75 ± 33	kHz kHz
Frequency Sweep Rates	10 250	kHz/sec Hz/sec
Power Level: High	42	dBm
Medium	33	dBm
Low	10	dBm

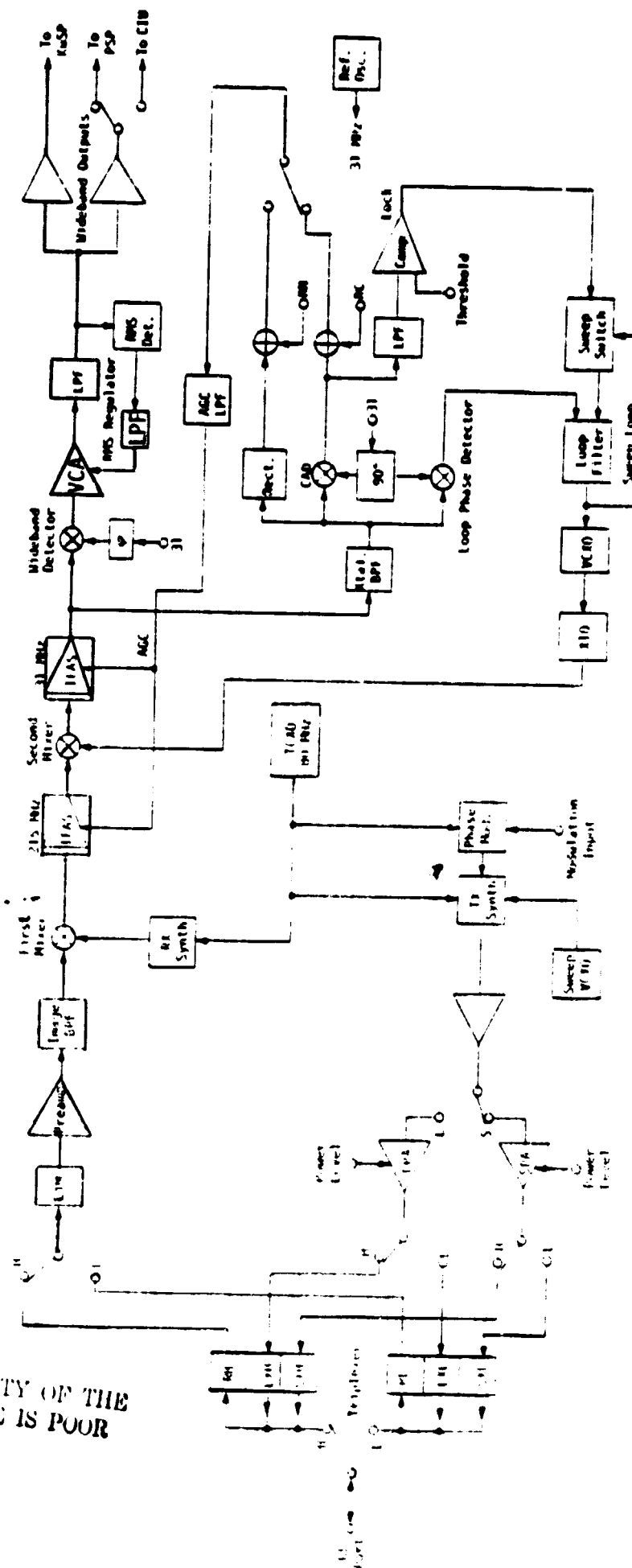


Figure 4.1. Payload Interrogator Functional Diagram

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limiter. This limiter functions to protect the FET preamplifier itself from any damage for applied power levels as large as +36 dBm. The preamplifier output is input through an image frequency-rejecting BPF to the first mixer.

The function of the first mixer is to downtranslate the received signal to a fixed intermediate frequency (IF) of 215 MHz. Since the input signal carrier frequency may correspond to any one of the designated channels on the range 2200-2300 MHz, the mixer reference supplied by the receiver synthesizer (RX) must also cover a 100-MHz range (1985-2085 MHz). Following the mixer is a wideband IF amplifier assembly (IFAS) consisting of several stages of gain-controllable (AGC) amplification and bandpass filters.

A second mixer further downconverts the 215 MHz first IF signal to the 31 MHz second IF. The reference for this second mixer is derived from the tracking loop VCXO, so the second mixer represents the input to a quasilong loop phase-locked loop (PLL) architecture. The second mixer is followed by an IFAS. At the output of the IFAS, the signal is effectively split into two principal channels.

The wideband channel provides for modulation recovery and output to the appropriate processing units. A wideband phase demodulator referenced to a 31 MHz oscillator (which becomes phase coherent with respect to the signal carrier component by virtue of the carrier tracking loop discussed subsequently) translates all of the signal first-order sidebands to the lowpass or baseband frequency region. The baseband waveform (which generally consists of signal-plus-noise) is then regulated to a fixed RMS value prior to being output.

A second 31 MHz channel is narrowband (approximately 30 kHz IF bandwidth) by virtue of the placement of a crystal BPF prior to two quadrature reference-driven demodulators. One of these demodulators, known as the loop phase detector, produces a carrier frequency/phase error voltage which is subsequently filtered and applied to the voltage control input of the PLL VCXO. The VCXO output is frequency multiplied by a factor of 10, whence it becomes the reference to the second mixer, thus completing the PLL circuit. For the conditions of proper PLL tracking, the frequency and phase of the received signal discrete carrier component at the input to the loop phase detector is in frequency-synchronous phase-quadrature with the 31 MHz derived reference.

Prior to achieving a condition of phase lock, the frequency difference between the received signal and the receiver references may be very large ($>\pm 100$ kHz). Thus, as an aid to attaining lock, the VCXO frequency is swept over the uncertainty range by means of the sweep loop. Once a state of lock is established, the sweep loop is disabled by the lock detector circuit.

The second demodulator of the narrowband quadrature pair is known as the coherent amplitude detector (CAD). If, when the PLL is locked, the input and reference to the loop phase detector have a 90° phase difference, the input and reference to the CAD have a 0° phase relationship. As a result, the CAD output is a direct (zero frequency) voltage with amplitude proportional to the level of the received carrier. Such a voltage has two distinct uses: (1) as a means of indicating phase lock, and (2) the basis for receiver automatic gain control (AGC).

To implement a lock detector, the CAD output is input to a two-pole small bandwidth LPF which is followed by a comparator referenced to a fixed threshold. When the PLL is out of lock, any direct signal component and noise voltage appearing at the LPF output are essentially smaller than the threshold so that the comparator output will indicate a "false" or out-of-lock status. Conversely, if the PLL is locked, the direct voltage appearing at the LPF output is sufficiently greater than the threshold so that the comparator output becomes "true", indicating a state of in-lock.

An AGC voltage is formed by simply offsetting the CAD output (i.e., adding a reference voltage, RC), lowpass filtering, and feeding the result back to the voltage-controllable gain amplifiers within the first and second IFAS's. Since AGC is also needed for receiver acquisition conditions when the PLL is out of lock and no direct voltage is produced at CAD output, a noncoherent AGC voltage is derived and used in this state. The implementation involves rectifying the 31 MHz output of the crystal BPF to obtain the AGC measure, adding a reference voltage RN, and switching the result into the AGC LPF (in lieu of the CAD output). Switching between noncoherent and coherent AGC is dependent upon which of the respective voltages is the largest (see section 4.1.5 for details).

Frequency synthesis for both the receiver and transmitter is based upon a master 80 MHz temperature-controlled crystal oscillator (TCXO). Transmitter carrier phase modulation takes place at a fixed frequency

which is subsequently translated to the proper output frequency within the transmitter synthesizer (TX). In order to frequency sweep the transmitter carrier, a VCXO sweep circuit is used, with its output also being input to the transmitter synthesizer. Thus, the output of the transmitter synthesizer is a discrete carrier, phase modulated and frequency swept signal with a nominal (no sweep) carrier frequency corresponding to the designated channel.

The transmitter synthesizer output is amplified to a level necessary to drive either of the output power amplifiers. Separate power amplifiers are used for L-band and S-band channels (respectively, LPA and SPA). Only one amplifier may be on or active at a given time. Either amplifier is capable of providing three selectable output power levels as listed in Table 4.2. Power amplifier output is switched into the appropriate triplexer subband.

Overall, the PI design philosophy is sound. The architecture, in terms of the frequency plan, appears to be excellent. Circuitwise, the triplexer, preamplifier, IFAS and transmitter power amplifiers are well designed and implemented with up-to-date (but conservative) technologies. The frequency synthesizers embody acceptable designs; however, their performance evaluation awaits future testing. Marginal (and potentially troublesome) designs (at least philosophically and, in some cases, due to circuit choices) exist in the phase-lock and frequency sweep functions. Detailed assessments are found in the following subsections.

4.1.2 Receiver RF and IF Circuits

4.1.2.1 Triplexer design and performance

Transco Products, Inc. is the subcontractor for the triplexer. Figure 4.2 is the triplexer functional diagram. A brief description of the triplexer design follows.

The triplexer consists of two sets (highband and lowband) of three filters. Each set has a receive filter, NASA (S-band) transmit filter and DOD (L-band) transmit filter. Either the highband or lowband set is selected or switched by means of four coaxial switches. The filters proper are implemented by means of cascaded cavities with adjustable resonators.

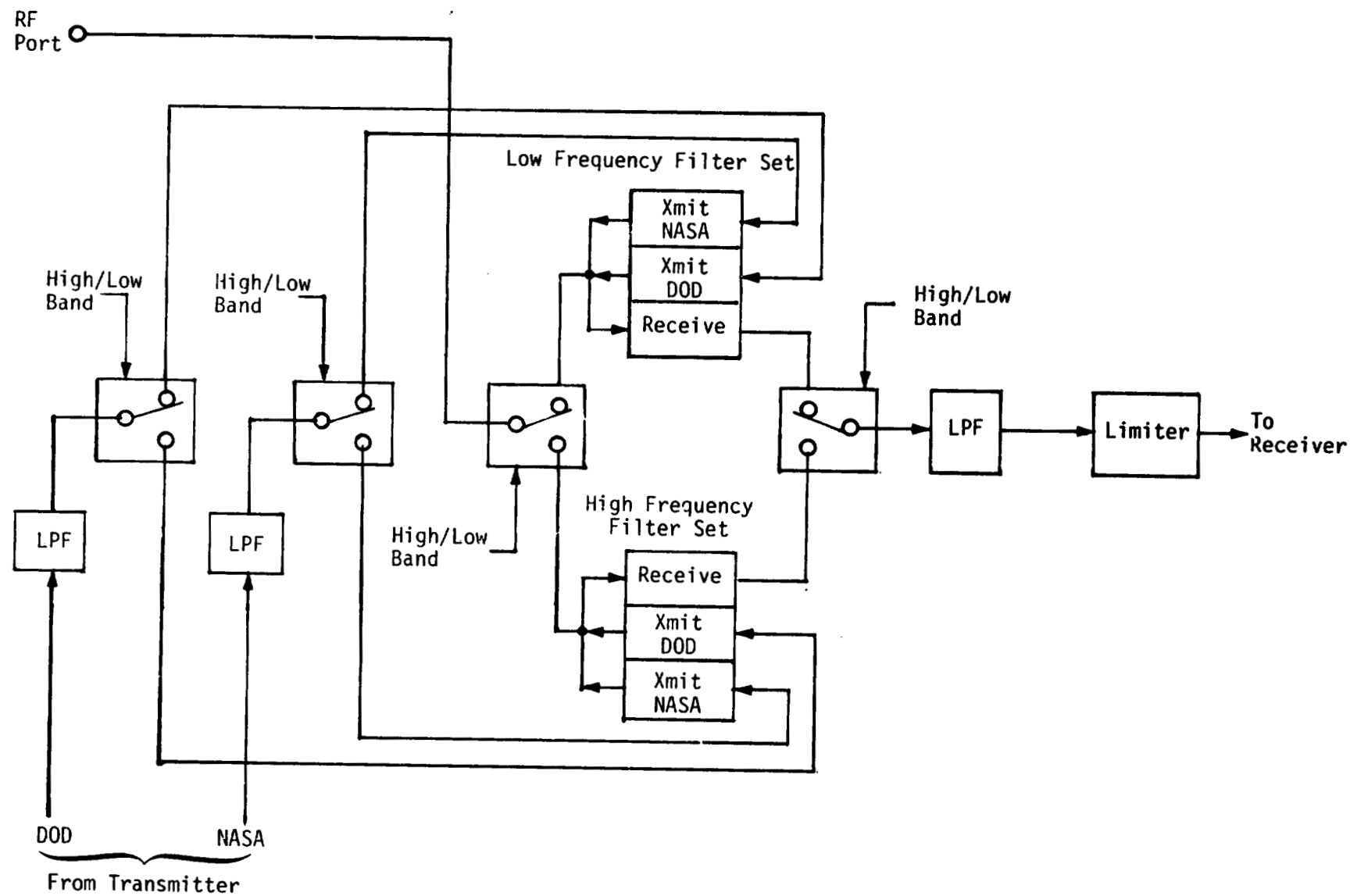


Figure 4.2. Triplexer Functional Diagram

Each filter channel utilizes high-Q combline structures with an integrated cross-coupled notch network to provide optimum electrical characteristics. Selection of the appropriate filter channel is provided by a switch matrix which is integrated into the triplexers without the necessity for external RF cables. Each switch utilizes an identical modification of a space-qualified design that allows integration without RF cables. Thus, the resultant insertion loss is reduced and the reliability is enhanced. Additionally, lowpass filters are incorporated into the three RF interfaces to obtain high stop-band attenuation up to 16 GHz.

The DOD and NASA transmit filters are of identical form in each band set. They embody, respectively, $N = 6$ and $N = 8$ resonator sections with elliptic-type response. $N = 8$ and $N = 10$ resonator sections with elliptic-type stop-band response are used for the respective low and high frequency receive channels. These designs have been chosen to provide the best possible amplitude response characteristics within the mechanical configuration constraints.

Each filter has been designed using exact synthesis techniques. The physical configuration consists of an aluminum block within which the individual cavities have been machined (or milled out). This block, called the housing, is designed for maximum efficiency. It provides sufficient wall/surface material for covers and components mounting while maintaining minimum wall thickness by a special undercut machining operation. This maximizes the unloaded Q , allows low insertion loss and minimizes weight. The entire housing is silver-plated.

The covers, together with the housing, form complete resonator cavities, and are also fabricated from an aluminum block and silver-plated. Resonator tuning is attained by adjustable capacitors for each cavity and constructed as shown in Figure 4.3. The capacitor posts and hats are fabricated from aluminum rods and silver-plated. Each resonator tuning screw is provided with a lock nut which is tightened after proper alignment is attained. It is also noted that the coupling to the filter non-common ports is capacitive and that coupling to the common junction (see Figure 4.2) is inductive.

The switches are mounted on the sidewalls of the housing with the actuating leaves projecting through the housing wall. Associated with each switch coil is an arc suppression diode, and all diodes are fixed to a common board which is also mounted to the housing sidewall.

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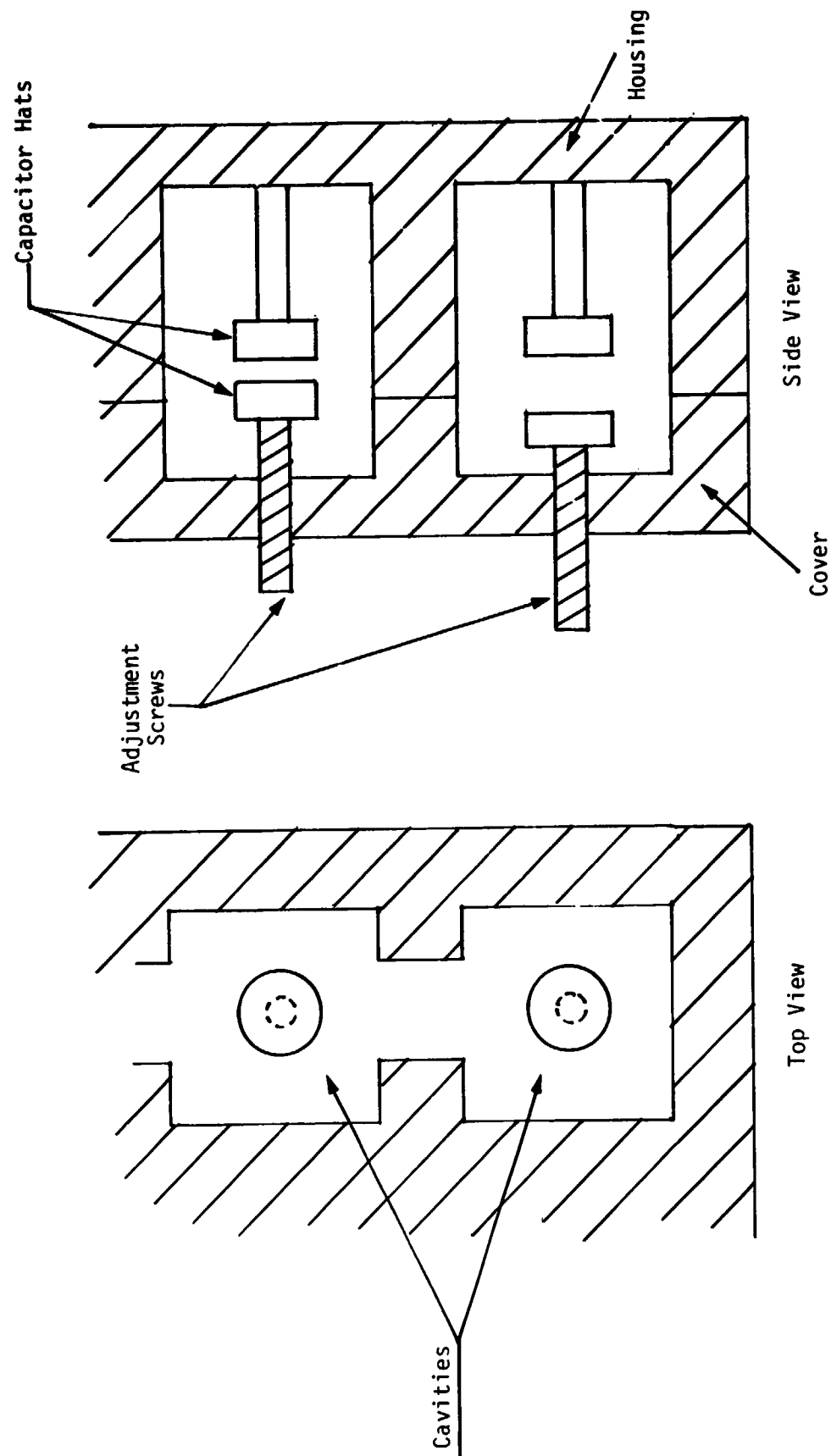


Figure 4.3. Cavity Adjustment Capacitors

Overall, the triplexer design, both electrically and mechanically, is judged very sound. The only potential mechanical problem is that the capacitor adjusting screws can be turned so that the two hats will make physical contact. This would appear to be a problem only during alignment and should be prevented by means of very careful procedures. It is believed that, once correctly adjusted, the capacitor hats have sufficient clearance to prevent contact due to temperature expansion or other mechanical stresses on the triplexer housing.

The mounting of the arc suppression diodes externally without a cover caused some initial concern over the possibility of EMI. However, considering that the triplexer will be mounted within the PI sealed housing and based upon some initial EMI measurements by Transco, there does not appear to be a problem.

Transco fabricated a brassboard triplexer and made performance measurements in order to verify the calculated design and obtain the data necessary for refining the engineering model design. The engineering model passband measured results are tabulated in Table 4.3.* In terms of the measured stop-band performance for the engineering model, both receive channels were within specification while the transmit channel filters were found to be outside of specification (worst case 5 dB) at certain high frequency points. These problems will be corrected by minor redesign of the lowpass filters and some resonator readjustments.

4.1.2.2 Power limiter and preamplifier

The triplexer design shown in Figure 8, page 54, of [1] had two fixed-pad attenuators capable of being switched into the circuit between the triplexer output and the preamplifier input so as to accommodate very strong received signals. As was pointed out on page 46 of [1], however, no operational criterion had been established as to how and when these attenuators should be set to the various options (0, -13 or -33 dB). Certainly they could not be relied upon as "burnout protection" for the preamplifier as there was no guarantee that they would be set at maximum attenuation when an excessively strong signal might be applied to the receiver input.

*The triplexer specified performance may be found on pages 53-59 of [1].

Table 4.3. Passband Performance Summary
PI Triplexer Engineering Model

<u>RECEIVE CHANNEL</u>	<u>REQUIREMENT</u>	<u>LOW FREQ</u>	<u>HIGH FREQ</u>
INSERTION LOSS	1.9 dB, max.	1.5 dB	1.4 dB
PASSBAND RIPPLE	± 0.2 dB, max.	± 0.1 dB	± 0.1 dB
PASSBAND VSWR	1.25:1 max.	$< 1.25:1$	$< 1.25:1$
<u>DOD TRANSMIT</u>			
INSERTION LOSS	1.7 dB, max.	1.1 dB	1.2 dB
PASSBAND RIPPLE	± 0.2 dB max.	± 0.1 dB	± 0.1 dB
PASSBAND VSWR	1.25:1 max.	$< 1.25:1$	$< 1.25:1$
<u>NASA TRANSMIT</u>			
INSERTION LOSS	1.7 dB, max.	1.2 dB	1.3 dB
PASSBAND RIPPLE	± 0.2 dB max.	± 0.1 dB	$< 1.25:1$
PASSBAND VSWR	1.25:1 max.	$< 1.25:1$	$< 1.25:1$

As the initial design of the triplexer evolved, it became clear to Transco and TRW that the attenuator pads and their associated coaxial switches were just too bulky to fit within the triplexer physical envelope specification. As a result, TRW sought to eliminate them in favor of an overload diode-type of limiter placed between the triplexer output and the preamp input. (Actually, this had been an earlier design approach that was abandoned by TRW when they believed that the limiter would significantly degrade the overall receiver noise figure. The subsequent selection of a very low noise FET input preamp minimized this objection.)

The use of a power limiter solves both the problem of operating the receiver at very strong signal levels and protecting the preamp against excessive input damage. Aertech Industries supplies TRW with both the limiter and the preamplifier, although the limiter is physically placed at the triplexer assembly and the preamp is contained within the first IF module. The preamp itself can tolerate up to +20 dBm without damage, whereas the maximum output allowed by the limiter is +13 dBm for any input power up to +36 dBm. Thus, a 7 dB safety margin exists.

The limiter begins to take effect at about a 0 dBm input. Mechanized using PIN type diodes, the limiter appears as a nonlinear resistor in shunt with the 50 Ω coaxial signal path. As a result, as maximum limiting takes place, a mismatch occurs, increasing the VSWR. However, this happens for signal levels higher than any operating value and therefore has no receiver operational impact. For input levels below the limiting threshold, the insertion loss is about 0.5 dB and the impedance is 50 Ω .

The preamplifier has between a 26 and 31 dB gain and employs input FET's to obtain a maximum noise figure (including the limiter) of 3.1 dB. Maximum 1 dB gain compression output power is specified to be +5 dBm.

Overall receiver noise figure, as seen at the source input, is determined by the preamp NF, plus insertion losses associated with the triplexer, cables and connectors. TRW calculates a combined component, worst-case, noise figure of 6.8 dB. The specified maximum value is 7.0 dB. Axiomatix has reviewed TRW's analysis and early test data, and believes that the projected NF maximum is correct and plausible.

4.1.3 Bandwidth and Transfer Characteristics

As of the PI PDR in October 1979, the modulation (carrier sidebands) transfer characteristics of the receiver were dependent upon the cascade of a number of filters within the receiver IFAS's. Figure 4.4 shows the various filter and amplifier cascades that comprise the receiver from the preamp through to the wideband output.

In designing the receiver frequency selective capabilities, TRW was concerned with simultaneously meeting two specifications: the first dealing directly with the wideband output 3 dB bandwidth, and the second implying roll-off or attenuation characteristics outside a central region about the carrier. These two specifications are (paraphrased):

- (1) The wideband output channel to the KuSP shall have a one-sided 3 dB bandwidth of 4.5 MHz
- (2) The presence of a -65 dBm signal, modulated or unmodulated, within the frequency regions outside of the carrier frequency ± 15 MHz shall not degrade the performance of the receiver by more than 1 dB.

Frankly, Axiomatix does not fully understand TRW's design philosophy or explanations offered for performance estimates. They maintain that, in order to meet the interference specification, (2) above, the first IF filters ($BPF_2 + BPF_3$) must have a minimum attenuation of -12 dB at ± 15 MHz from center frequency. However, TRW's analysis (see subsection 4.23.2, page 4-165 of the PDR Data Package, Vol. I) and Axiomatix's analysis (see section 5.2, pp 59-66 of [1]) of the interference degradation mechanism do not include the skirt responses of the IF filters as they have no effect on the problem. Yet, when TRW was asked (by Axiomatix) why they cannot widen certain IF filters, their response has been that they can if the interference specification is relaxed somewhat. At this point, it must be noted (as was previously done on page 66 of [1]) that TRW originally misread the interference specification in that they took the degradation to be -0.1 dB rather than -1.0 dB. Thus, a 14 dB margin on equivalent noise spectral density generated by the interference already exists; no specification relief therefore appears necessary.

Turning now to the central problem created by the current receiver filter design, Table 4.4 lists the parameters for the filters identified on Figure 4.4. As may be seen, the narrowest filter that

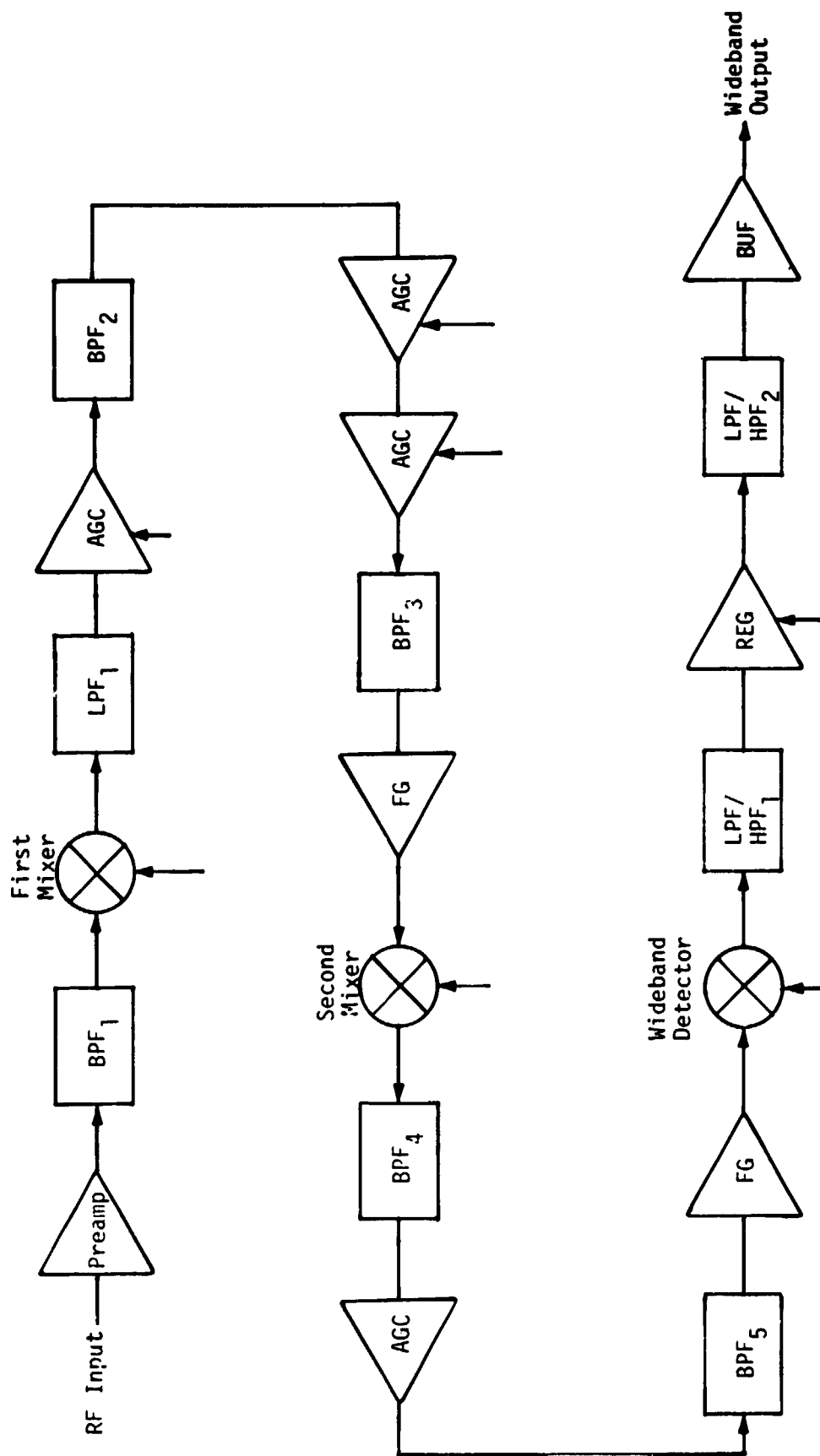


Figure 4.4. PI Receiver Amplifier and Filter Cascade

Table 4.4. PI Receiver Principal Filter Parameters
(Refer to Figure 4.4)

Filter Designation	Nominal Center Frequency	Number of Poles	-3 dB Bandwidth
BPF ₁	2250 MHz	3	150 MHz
LPF ₁	215 MHz	3	600 MHz
BPF ₂	215 MHz	5	18 MHz
BPF ₃	215 MHz	5	18 MHz
BPF ₄	31 MHz	3	31 MHz
BPF ₅	31 MHz	3	12 MHz
LPF/ HPF ₁	Baseband	2 1	12 MHz 400 Hz
LPF/ HPF ₂	Baseband	2 1	8 MHz 700 Hz

should predominate the wideband output bandwidth is BPF_5 , which has a two-sided IF bandwidth of 12 MHz or a one-sided lowpass equivalent bandwidth of 6 MHz. Now, TRW's design philosophy is that the 4.5 MHz lowpass 3 dB bandwidth is met by the cascade of all filters listed in Table 4.4. Thus, each filter contributes more or less and, when each and every filter is represented by its nominal parameters, the 4.5 MHz is attained. The problem is that, with temperature and other variations (aging and manufacturing tolerances), each filter either shifts its center frequency (some upward and some downward) or detunes, to the effects that, under worst-case conditions, the cascaded response may be as large as 8 MHz. A nominal bandwidth on the order of 6 MHz can be expected.

Axiomatix does not understand why some of the IF filters cannot be widened, especially BPF_2 , BPF_3 and BPF_5 , and the baseband LPF/HPF filters narrowed so that these latter filters predominate and effectively establish the wideband output bandwidth. Since the baseband filters are RC types, they are much less subject to temperature changes and aging and manufacturing tolerance variations than are the IF filters. Such, in lieu of additional qualifying factors, is Axiomatix's recommendation.

4.1.4 Wideband Output Regulation

As was indicated in subsection 3.2.6, a wideband output RMS type of regulating loop was selected based upon economic considerations. Axiomatix's preference and recommendation prior to the decision was that the regulating loop be of the signal-peak type (see 5.4.1, pp 134-142 of [2]). This was based upon the fact that the peak regulator optimizes the Ku-band link FM deviation for all types of waveforms, providing maximum bent-pipe SNR performance for all waveform conditions. The RMS regulator, on the other hand, may have its output scaled to provide optimum deviation for any chosen waveform, but the deviation for all other waveforms will be suboptimum. If, for example, the RMS regulator output is optimized for the Gaussian waveform (characteristic of PI low SNR conditions), the FM transmitter will be underdeviated for all other waveforms (high SNR conditions). Table 4.5 lists the FM transmitter mean deviations for the two types of regulators and various waveforms.

In addition to wanting optimum mean deviation, there is some maximum deviation (set by specification and design) which can be allowed. Again, the peak regulator always satisfies the maximum deviation criterion

Table 4.5. Bent-Pipe FM Transmitter Mean Deviations (MHz)

	RMS Regulator	Peak Regulator
One Sinusoid	3.7	7.8
Two Sinusoids	3.7	5.5
Three Sinusoids	3.7	4.4
Four Sinusoids	3.7	3.9
Square	3.7	11.0
Gaussian	3.7	3.7

but the RMS regulator may not. The maximum deviation for the bent-pipe transmitter is 11 MHz. Now suppose the RMS regulator is used and its output is scaled to provide optimum deviation for a single-sinusoidal waveform. From Table 4.5, the mean deviation will be 7.8 MHz. If a Gaussian waveform rather than the single sinusoid then appears at the input to the RMS regulator, the RMS regulator will automatically scale the Gaussian waveform to cause a mean deviation of 7.8 MHz. But the peak-to-peak to RMS ratio of a Gaussian waveform is on the order of 3:1; therefore, the peak deviation will be 23.4 MHz, or more than two times larger than the maximum deviation limit.

To prevent overdeviation, an amplitude clipper is usually employed at the input to the FM transmitter. Thus, for the Gaussian waveform example just cited, it would be clipped at its 1.4σ level, causing distortion and SNR loss. For the specified performance finally agreed upon (see 3.2.6), the nominal clipping level should be 1.75σ , and worst-case, 1.46σ . TRW's RMS regulator design and performance is now reviewed.

Figure 4.5 is a block diagram of the wideband output regulator. Regulation error is generated by the RMS detector relative to a voltage reference, and signal drive correction to the IC video amplifier is made via the voltage-controlled variable attenuators. The attenuators are

simply two L-pads with the shunt arms being formed by FET's which function as voltage-variable resistors. Overall, the regulation loop design is sound.

Two observations concerning the regulator performance are made. The first is that the tolerances for temperature, production and aging are such that a ± 0.34 V variation of a 2.0 V RMS sine wave can be expected. This is within specification.

The second comment is that the RMS detector does not have a true RMS characteristic with respect to all waveforms. Measurements made on the breadboard established that, if, for a sine wave, the nominal output is 2.0 V RMS, for a square wave it will be 1.93 V RMS, and for 6 MHz lowpass noise, the output will be 2.33 V RMS. Table 4.6 tabulates the expected RMS output for true RMS ($v=2$) and true linear ($v=1$) characteristics for comparison with TRW's measurements. It is seen that, for a square wave, the regulator is between linear and RMS, while the Gaussian (noise) waveform case would appear to act as $v<1$ (although it is expected that compound nonlinearities obscure the actual detector characteristics). The net result of the TRW performance characteristic is that bent-pipe FM performance will be even more suboptimum than for a true RMS regulator, which has already been established as significantly suboptimum relative to a peak regulator for the case of square wave (data) signals (see Table 4.5).

Table 4.6. Regulator Characteristic Comparison

Waveform	Nominal RMS Output (Volts)		
	True RMS ($v=2$)	True Linear ($v=1$)	TRW Characteristic
Gaussian	2.00	2.24	2.33
Sinewave	2.00	2.00	2.00
Squarewave	2.00	1.82	1.93

TRW states that, by individual unit adjustment, the $+0.33$ V change when going from a sine wave to noise can be reduced to $+0.25$ V. Thus, the overall tolerance on a noise waveform will be ± 0.59 V. Taking the worst-case positive tolerance value of the regulator output to be 2.59 V RMS, the peak clipping to RMS ratio of the noise will be 1.35σ . This means that the noise will be clipped a fair percentage of the time. The estimated SNR degradation due to this process is about -0.2 dB.

4.1.5 AGC Design

Figure 4.1 shows that the receiver AGC loop switches between the coherent (CAD) and noncoherent (rectifier) sources. The method by which this is actually accomplished is shown in the circuit of Figure 4.6. Diodes D_C and D_N act as the switch. When the PLL is out of lock, the direct voltage output of the CAD is zero and, because of the 8.2 V zener bias established by the coherent AGC amplifier, the diode D_C is reverse biased (switch open). On the other hand, the AM detector (rectifier) produces a voltage which the overall AGC loop seeks to maintain constant. The noncoherent AGC amplifier output is such that diode D_N is forward biased (switch closed).

Now when PLL lock is attained, the CAD output is sufficient to close the switch D_C . Further, in order to totally disable the noncoherent AGC (i.e., open D_N), the lock detector output (COMP output) is switched into the noncoherent AGC amplifier, with the result that diode D_N is forced to a reverse-bias state irrespective of the AM detector input level. Thus, the noncoherent AGC voltage makes no contribution to the receiver gain control function when the receiver is in lock.

The design of the AGC loop and coherent/noncoherent switching circuits is both proper and practical. In discussing the design with TRW's engineers, Axiomatix noted that the effective noise bandwidth of the AGC amplifiers (they have a unity gain plus proportional integral transfer characteristic with regard to their + inputs) is large. TRW had observed this fact in the breadboard testing and has since decided to incorporate an additional AGC LPF within the overall loop. The location of this filter is shown in the upper right-hand corner of Figure 4.6.

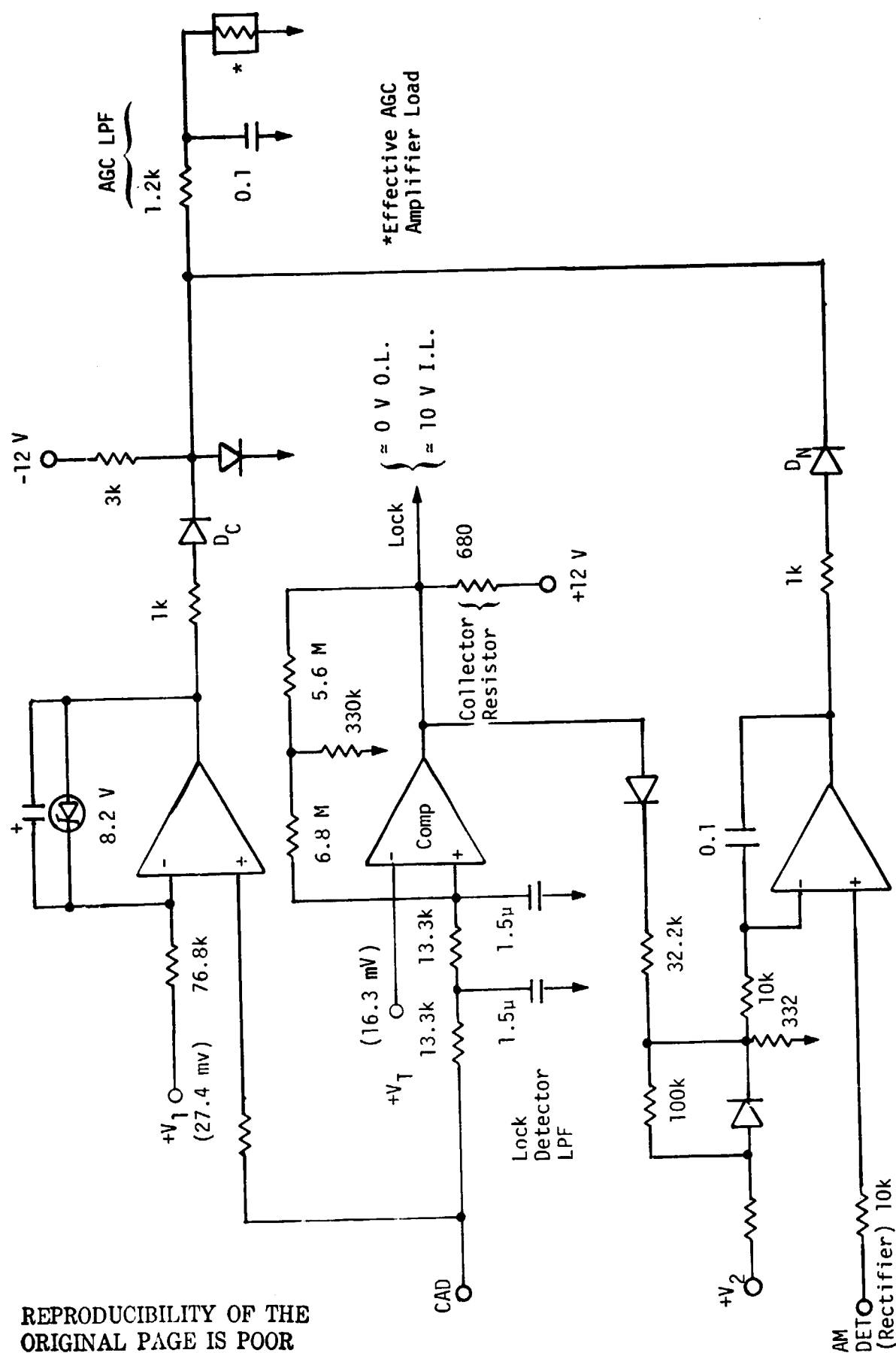


Figure 4.6. AGC and Lock Detector Amplifier Configuration

4.1.6 Tracking Loop Design and Performance

It is stated at the onset to this subsection that the circuit designs for the PLL filter and sweep functions are, in Axiomatix's opinion, some of the least acceptable found within the PI. The primary problem is centered on the fact that a single operational amplifier, whose configuration zero-frequency gain is equal to the amplifier open-loop gain, is used both for the PLL second-order loop filter and to generate the receiver frequency sweep sawtooth waveform. Figure 4.7 shows the functional aspects of the active circuit configuration.

The loop filter time constants are $\tau_1 = R_1 C$ and $\tau_2 = R_2 C$. In open loop, the PLL will have a gain of GK , where G is the zero frequency gain of the LM 108 operational amplifier (about 110 dB), and K is the remainder of the PLL loop gain and comprises the phase detector sensitivity, the VCXO transfer gain, the frequency multiplication factor ($\times 10$), and any miscellaneous gain (or loss). For the current TRW design, $GK \approx 5.1 \times 10^9$.

One good feature of the loop filter configuration is that the time constant τ_1 depends only upon the gain K and not the gain GK . Thus, the resistor and capacitor values are of reasonable electrical size. Further, the very large open-loop gain, GK , forces the loop static phase error (SPE) for very large frequency error to be quite small. For example, when the tracked frequency error is 100 kHz, the SPE will be only 0.007° . Although this appears to be quite commendable (in fact, it is over design), there is an equivalent price paid in terms of amplifier offset voltage and currents and their drift with temperature and aging. Generally, the higher the amplifier gain, the larger the output offset voltage. Therefore, when the operational amplifier has no effective feedback at zero frequency, the output offset voltage can be expected to be large. TRW reports that the equivalent SPE due to offset voltage is expected to be 8° . What is meant by this is that the phase detector must generate a cancelling voltage at its output in order to maintain a proper phase lock condition.

It is educational to calculate what just a little zero frequency feedback stabilization around the operational amplifier might accomplish. Suppose that a resistor, R_3 , were connected across the operational amplifier as shown in Figure 4.7. Assuming, for the sake of example, that

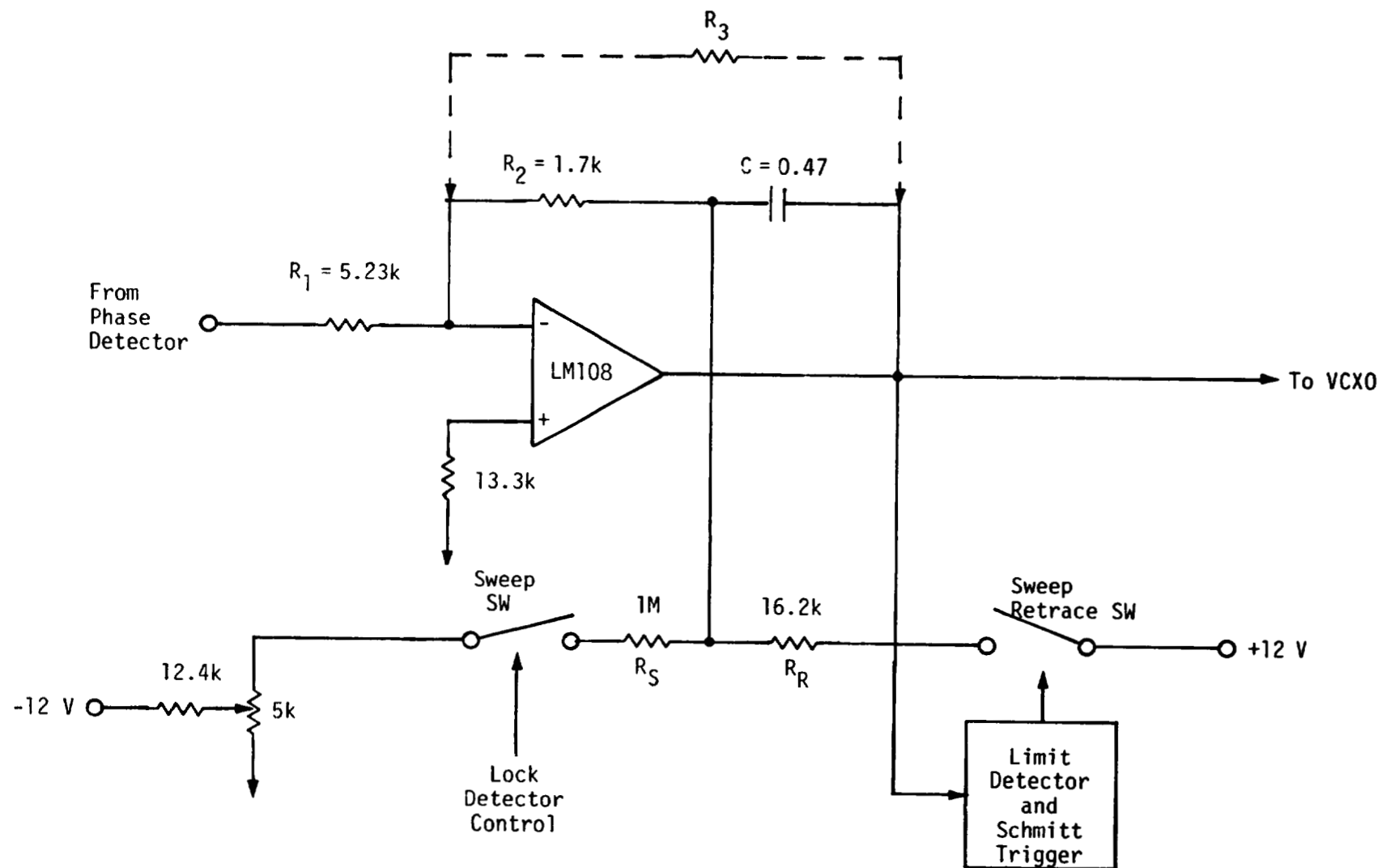


Figure 4 7. Loop Filter and Sweep Circuit

all of the output offset voltage is due to an input offset multiplied by the gain, G , of the amplifier, the relationship between the input and output offset voltages is:

$$V_{\text{offset}} = \left[1 + \frac{R_3}{R_1} \frac{1}{1 + (1/G)(1 + R_3/R_1)} \right] V_0 \quad (4-1)$$

Now, when $R_3 = \infty$,

$$V_{\text{offset}} \cong [1 + G] V_0 . \quad (4-2)$$

However, let R_3 now be chosen so that $R_3/R_1 = G/100$. Then,

$$V_{\text{offset}} \cong \left[1 + \frac{G}{100} \right] V_0 . \quad (4-3)$$

The result is that the zero frequency gain is reduced by a factor of 100, but so is the output offset. This will correspondingly reduce the offset voltage equivalent SPE to (ideally) 0.08° . At the same time, the SPE due to the maximum tracked frequency error will increase from 0.007° to 0.7° , so that the overall SPE from both effects will be about 0.8° . In reality, the improvement will not be quite so pronounced as not all of TRW's 8° SPE equivalent error is generated by the subject amplifier. The point is, however, there exists a feedback constrained gain which minimizes the overall SPE effects, and TRW should determine the best value for R_3 and include R_3 in their circuit.

The second major concern is the method for implementing the sweep voltage and control circuits. Viewed from the sweep perspective, the configuration of Figure 4.7 acts as an operational integrator having two switched time constants, $R_S C$ and $R_R C$. With the sweep retrace switch open and the sweep switch closed, the output of the operational amplifier is a positive slope ramp that begins nominally at $-V_S$ and increases to $+V_S$. When the $+V_S$ limit is reached, the limit detector and Schmitt trigger assembly close the sweep retrace switch which connects the $+12$ V source into the circuit through the short-time constant ($R_R C$), forcing a rapid return to the $-V_S$ voltage. This limit is detected and the sweep retrace switch opened, at which point the cycle repeats.

The sweep rate or ramp slope is affected by (1) the R_5C time constant, and (2) the effective charge source voltage (set by the 5 k Ω pot). In addition, the total sweep limits are established by the accuracy of the limit detecting Schmitt trigger. This latter circuit is mechanized using a type 741 operational amplifier connected in a positive feedback configuration. Since TRW has not, to date, documented the design (especially the Schmitt trigger circuit), it is not at all clear to Axiomatix why they selected this particular approach. (Axiomatix believes a number of superior and less potentially troublesome designs should have been studied.) The concern is with the performance variations that may be expected with temperature, aging and power supply changes. Further, there are three pots that must be adjusted* in order to bring the circuit parameters within operating specifications. It can only be wondered that there will not be trouble encountered with the flight units. The design appears to be too dependent on small tolerance component values and perhaps critical adjustments. Axiomatix therefore suggests that potential failure mechanisms be identified and evaluated. Since the receiver false lock performance is dependent upon maintaining a proper sweep rate (see section 4.1.7 following), any circuit changes which can cause the rate to fall outside its prescribed limits (either too fast or too slow) are potential failure mechanisms. Also, failure of the Schmitt trigger to switch when either sweep limit is reached is a failure which will render the receiver essentially inoperative.

4.1.7 Acquisition and False Lock Susceptibility

A background for the problem of swept acquisition lock on carrier modulation sidebands (called false lock) is found in [1], pp 66-75. From the time that [1] was written in January 1979 to the PI PDR held in early October 1979, the philosophy used by TRW to abrogate false lock changed significantly.

TRW's old approach was to sweep the PI receiver tracking loop VCO frequency at a moderately slow rate (10 kHz/second) and rely on the discriminating performance of the lock detector to indicate carrier lock

*An examination of the schematic diagram for the circuit board of the phase lock and telemetry assembly discloses that no less than six pots are available for alignment, three for the sweep circuit, one for the AGC and two for the AGC telemetry.

(and thus disable the sweep) but not indicate sideband lock. As a result, accurate receiver gain control in both the out-of-lock and in-lock phases was essential, as a single fixed lock detector threshold voltage was employed. A very serious problem with this old approach was that, at strong signal conditions, the beat note frequency between the received carrier and the receiver effective reference could, if the lock detector lowpass bandwidth were large, cause the sweep to be terminated before the beat note frequency had become sufficiently small to allow the phase-locked loop to self-capture. As a result of these problems, the acquisition performance was difficult to analyze.

The new method allows the receiver frequency sweep to be very fast--sufficiently rapid that sideband lock is obviated--but not so fast that true carrier lock is compromised or uncertain, even at threshold SNR's. Furthermore, the lock detector lowpass bandwidth is rather narrow (approximately 4 Hz, see Figure 4.6), thereby eliminating the beat note problem. It should be noted that, from both conceptual and theoretical perspectives, the new approach is the correct one (as Axiomatix had advocated when sideband lock first became an issue).

TRW now bases the selection of the PLL parameters on maximizing the acquisition sweep rate. Thus, the largest PLL natural frequency allowable is desired. A minimum PLL SNR of 6 dB corresponding to acquisition carrier threshold of -122.5 dBm is specified by TRW. Taking a receiver maximum noise figure of 7 dB and allowing a 2 dB margin for implementation losses, a receiver noise bandwidth ($2B_L$) of about 3230 Hz is calculated, which corresponds to a PLL natural frequency of $\omega_n = 2560$ radians/second (loop damping factor slightly larger than unity).

Although TRW calculates the maximum allowable sweep rate for 0.9 probability of acquisition on the true carrier when the PLL SNR is 6 dB, they have found by running tests on the breadboard that the theoretical sweep rate is too fast for reliable performance. Gardner's formula ([3], equation 4-33) gives

$$f_{sw}(\max) = \frac{[1 - (\text{SNR})_L^{-1/2}] \omega_n^2}{2\pi}, \quad (4-4)$$

which, for the above stated conditions, results in $f_{sw}(\text{max}) = 520 \text{ kHz/s}$. TRW's experimental investigations have determined, however, that $f_{sw} = 330 \text{ kHz/s}$ is the practical rate. This number includes allowance for the received signal carrier sweep of 17 kHz/s which could add directly to the receiver local sweep, tolerances and some acquisition margin (not delineated by TRW).

Axiomatix had previously established that the ratio of sideband to carrier amplitude given by

$$\frac{J_1(\beta)}{J_0(\beta)} < \frac{\omega_{sw}}{\omega_n} \quad (4-5)$$

will theoretically preclude false lock. Calculating the ratio for $f_{sw} = 330 \text{ kHz/s}$ and TRW's largest expected value of $\omega_n = 2923 \text{ rad/s}$ results in an answer of $< -12.3 \text{ dBc}$. This result assumes, however, that both the carrier and the sideband levels remain relatively unaltered irrespective of the frequency error or sweep process. In reality, such is not the case as, for large frequency errors, the carrier may actually be attenuated by the skirts of the crystal IF filter. When this happens, the non-coherent AGC increases the receiver gain so that ω_n also increases. Thus, allowance must be made for this condition. In their analysis presented in the PI PDR Data Package, Vol. I, page 4-36ff, TRW accounts for this phenomenon in an unacceptable (and difficult to comprehend because of its sketchiness) manner. Their predictions, especially those dealing with extrapolations from measured breadboard results to flight unit expected performance on page 4-37, should, in Axiomatix's opinion, be disregarded. TRW's breadboard measurements showed that false lock would not occur if the sideband level were $< -23 \text{ dBc}$. This is over 10 dB different from the limit calculated using equation (4-5). Although several dB of this difference can be accounted for due to the aforementioned crystal filter effect and tolerances, the remainder is unexplained. At this point, Axiomatix feels that more careful measurements should be taken and that further analytical development is needed. The matter of resolution and predicted performance for the flight units therefore remains open.

4.1.8 Frequency Synthesis

Figure 4.8 is a simplified functional diagram of the PI frequency synthesizer. The principal frequency source is the temperature-controlled crystal oscillator (TCXO) having an output frequency of 80 MHz.

Frequency output of the receiver synthesizer portion is given by

$$f_{Rx} = \left[160 \frac{N}{D} + 1920 \right] \text{ MHz} , \quad (4-6)$$

where N is a frequency division integer that establishes the desired channel frequency and D is the interchannel step size scaling factor. N and D are tabulated in Table 4.7 for the various payload options.

Table 4.7. Synthesizer Integer Values

Integer	STDN	DSN	SGLS
N	CN + 519	CN - 431	40CN - 35460
D	1280	432	1280
E	240	240	256
F	221	221	205
CN = Channel Number			

The transmitter output frequency is either S-band (STDN/DSN) or L-band (SGLS) and is given respectively by:

$$\text{(S-band)} \quad f_{Tx} = \left[160 \frac{NF}{DE} + 10 f_{VS} + 1280 \right] \text{ MHz} \quad (4-7)$$

$$\text{(L-band)} \quad f_{Tx} = \left[160 \frac{NF}{DE} + 6 f_{VL} + 1280 \right] \text{ MHz} \quad (4-8)$$

here the ratio F/E is the payload transponder receive-to-transmit frequency ratio (see Table 4.7), and f_{VS} and f_{VL} are, respectively, the S-band and L-band sweep VCXO nominal frequencies.

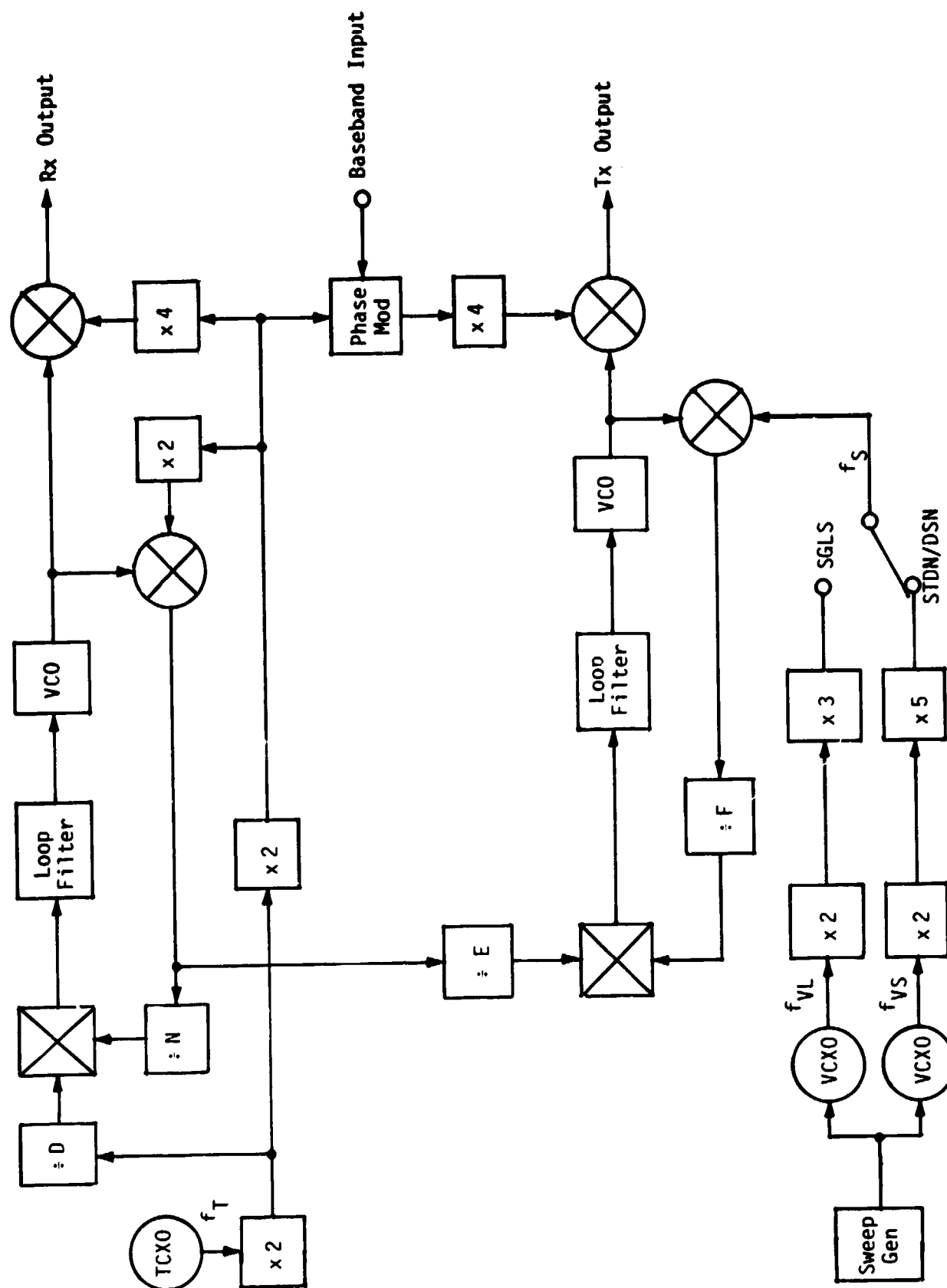


Figure 4.8. PI Frequency Synthesizer

Channel frequency synthesis is implemented using an indirect phase-lock method. TRW has done a good job with respect to design detail and analysis. Because the changes of integer values directly affect the PLL loop gain, TRW has placed a three-position attenuator in the loop following the loop filter. This attenuator, automatically switched according to the channel number selected, holds the PLL natural frequency within prescribed variation limits (about ± 3 dB) over the entire set of channels. TRW makes use of a rather novel PLL phase detector (identified as the FSP-1X), which produces a direct voltage output as a function of both frequency error and phase error (when the two input frequencies are identical). This is a very important feature when it is considered that the loop is required to frequency-slew as much as 100 MHz (e.g., from Channel 1 to Channel 808 in the STDN mode). Without some form of AFC acquisition, the basic PLL cannot accommodate such frequency steps and self-acquire. The combination frequency/phase error characteristics also diminishes the possibility of false lock. Another good performance feature is that the loop is designed to operate in the in-lock state with an intentional phase error. This property avoids the generation of "digital" phase noise which occurs at the phase detector output within the vicinity of 0° phase error.

One concern of Axiomatix has been the phase noise output of both the transmitter and receiver synthesizers. Most of the receiver synthesizer phase noise may be traced back to the inherent instability of the TCXO. If the TCXO has a phase noise modulation denoted by $\theta_T(t)$, the receiver synthesizer output has a phase noise given by

$$\theta_{RX}(t) = 2\left(\frac{N}{D} + 12\right) \theta_T(t) . \quad (4-9)$$

This has a maximum value of $\theta_{RX}(t) \approx 26\theta_T(t)$. The transmitter, on the other hand, has phase noise components derived from both the TCXO and one of the VCXO's and, for the STDN mode, the transmitter phase noise is

$$\theta_{TX}(t) = 2\left(\frac{NF}{DE} + 8\right) \theta_T(t) + 10 \theta_V(t) \quad (4-10)$$

where $\theta_V(t)$ is the phase noise modulation of the VCXO. The maximum value is $\theta_{TX}(t) \approx 16\theta_T(t) + 10\theta_V(t)$. In addition to the crystal oscillator sources cited, other phase noise components arise from the synthesizer PLL VCO's and the frequency division and phase detector circuits. All of these latter components tend to make their greatest contributions outside of the synthesizer PLL bandwidth, i.e., $>\pm 4$ kHz from the nominal carrier frequency. Most of the phase noise data supplied by TRW to date has been taken from breadboard measurements and is both sketchy and somewhat imprecise (due to the limitations of the test equipment available). One possible performance problem is that the phase noise spectral density of the receiver synthesizer ± 15 MHz from the nominal frequency may be some 3 dB greater than that needed to meet the -65 dBm interference degradation specification. Axiomatix has requested refined phase noise measurements of both the transmitter and receiver synthesizer outputs.

Probably the poorest circuit design found in the entire frequency synthesizer is the sweep generator. The sweep waveform (triangular) is obtained from circuits not unlike those already described for the receiver sweep (see section 4.1.6). An operational integrator utilizing an LM108 amplifier is employed in conjunction with an LM139 voltage comparator which detects the ramp limits. By the use of an integrator input polarity reversal switch and comparator reference value switches, a triangular waveform which begins at 0 V, increases to +4 V, reverses and decreases to -4 V and reverses again to return to 0 V, is generated.

The most critical problem associated with the sweep circuit design is that, at the slow sweep rate (250 Hz/s), the nominal integration period (+4V to -4 V) is some 246 s. Because of operational amplifier offset voltage and current drifts over such a rather long time, TRW can meet the slow sweep rate with a tolerance of no better than $\pm 30\%$. Nor will the sweep be perfectly linear over the entire period.

As a result of the sweep circuit design philosophy, no flexibility outside of providing two distinct rates has been possible. One desirable feature would be to begin the sweep at the -4 V limit, increase to +4 V, reverse and decrease to 0 V. This would save 25% of the time required to make the sweep cycle (important at the slow rate). Still another capability could be the starting of the sweep at any prescribed value and ending (and holding) at a second value. Such would allow for

a priori knowledge of the probable payload receive frequency to be used to significantly shorten the acquisition time at the slow rate. In order to accommodate such capabilities, an entirely different sweep design must be employed. An approach would make use of an up/down counter which could be set and stopped at any preprogrammed limits, a variable/selectable counter clock frequency, and a digital-to-analog converter having an interpolative step filter. Not only can flexible sweep profiles be generated by such a mechanization, but the tolerance problems associated with slow ramps are virtually eliminated. Further, a large number of sweep rate options are possible by simply changing the counter clock frequency through a programmable divider operating from a master clock source. Therefore, Axiomatix recommends that, whenever some future PI redesign/upgrade program is initiated, the suggested approach be adopted to replace the analog operational-integrator method. (This recommendation also applies to the receiver sweep circuits.)

4.1.9 Transmitter Power Amplifier

The transmitter power amplifier is an excellent example of modern solid-state design using distributed microstrip technology, together with parallel combining of the power transistors using hybrid coupling. Emphasis has been given to efficiency and the problem of heat dissipation. Detailed, well-written, descriptions of the design and performance are given in the TRW PDR Data Package, Vol. I.

It is instructive to briefly review the method by which the three power levels are obtained. Figure 4.9 shows the power switching configuration along with the PIN diode switching matrix. The input is nominally 4 W at node A. In the high-power mode, the 4 W is split (insertion loss is ignored in this simplified discussion) into 2 W at each power amplifier (PA) input; little significant power is reflected to port B. Each PA produces about 8 W at its output, with the combination appearing as 14 W at the output node D. In the medium and low-power modes, the PA's make no contribution to the output as the PIN diodes at their inputs and outputs are shorted, thus providing reflective loads to the hybrid ports. As a result, the power incident at A is reflected to B, from whence it is transferred to point C via the lower leg in the medium-power mode, or to point C through the power attenuation leg in

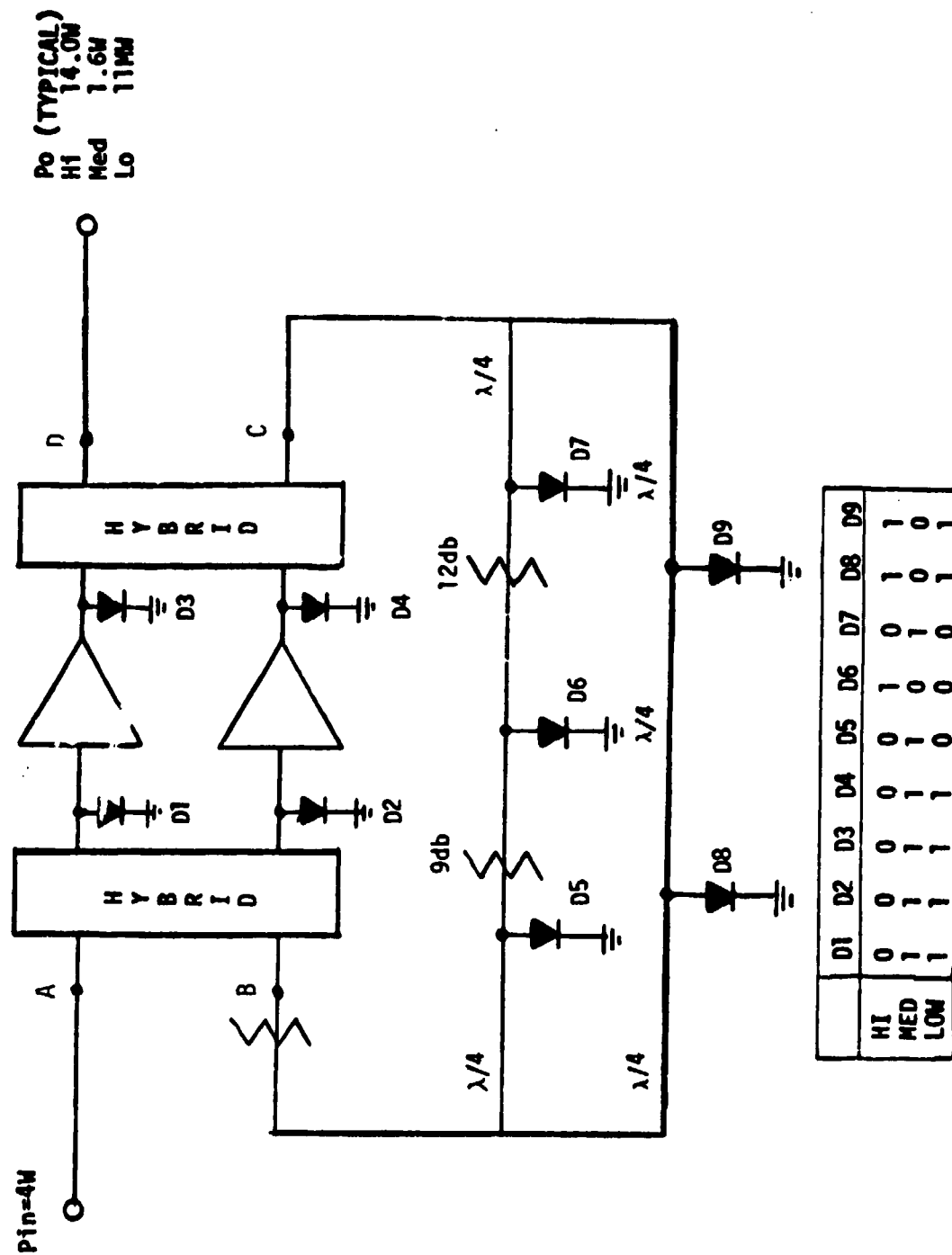


Figure 4.9. Power Switching Block Diagram, Reflective Hybrid Switching

the low-power mode. Power incident at node C is reflected to node D (because of the shorted diodes), thereby completing the circuit to the output.

Performance of the breadboard power amplifier is summarized in Table 4.8.

Table 4.8. Power Amplifier Breadboard Performance

Mode	Output Power	
	Measured	Specification
High	40.6 - 42.2 dBm	40.2 - 43.5 dBm
Medium	30.9 - 33.5 dBm	30.2 - 33.5 dBm
Low	10.5 - 12.8 dBm	7.2 - 10.5 dBm
Spurious Products	≤ -70 dBc	≤ -67 dBc

4.1.10 Receiver Performance Assessments

Based upon TRW's analysis and breadboard receiver test results, Axiomatix has made the following determinations.

In terms of acquisition and tracking thresholds, breadboard measurements have established the absolute acquisition threshold carrier value ($P_{ACQ} = 0.9$) to be -127.2 dBm and the tracking threshold carrier level to be -130.0 dBm (mean time to loss of lock equal to 10 s). Since the breadboard tests do not include the front-end loss of up to 2.9 dB due to triplexer, cables and connectors, this must be accounted for. Table 4.9 tabulates the expected and specified performance. The margins shown would appear, at this point, to be adequate for allowances or degradation that may occur in the flight units due to tolerance and manufacturing variations.

As regards throughput performance, Axiomatix had previously identified the component loss parameters, and TRW has also established most of them by means of analysis and testing. Axiomatix's evaluation

Table 4.9. PI Receiver Carrier Threshold Performance

	Measured	Specified	Margin
Acquisition Threshold	-124.3 dBm	-122.5 dBm	1.8 dB
Tracking Threshold	-127.1 dBm	-124.0 dBm	3.1 dB

of these losses appears in Table 4.10 for both standard and nonstandard (bent-pipe) modulations. For the standard modulation case, the margin, by design, is small and a reasonably high confidence prevails that the flight units will attain the indicated level of performance. As for the nonstandard modulations, the rather large filtering loss is based upon the possibility that the receiver throughput bandwidth could be as narrow as 3 MHz (see the discussions under 3.2.5 and 4.1.3). This is a worst-case estimate and could improve by better than 0.5 dB if a bandwidth closer to the 4.5 MHz specified value is attained.

Table 4.10. Anticipated PI Receiver Throughput Losses

Component	Standard Modulation	Nonstandard Modulation
Filtering	-0.2 dB	-1.0 dB
Interference	-1.0 dB	-1.0 dB
Tracking and Phase Noise	-0.5 dB	-0.5 dB
Nonlinear	-0.2 dB	-0.4 dB
Total	-1.9 dB	-2.9 dB
Allocation	-2.1 dB	-2.1 dB
Margin	+0.2 dB	-0.8 dB

4.2 Assessment of the PSP Design and Performance

TRW held a preliminary design review for the Payload Signal Processor May 2-3, 1979. A design data package and the viewgraphs used at the formal presentation were distributed. In the subsections that follow, Axiomatix presents its assessment of the PSP design, performance and potential problems.

4.2.1 Overall Philosophy

The PSP consists of two basic processors--one to handle telemetry data and the second to process and encode command messages. Telemetry input is in the form of data biphase modulated onto a subcarrier which is serially processed in such a manner as to (1) PSK demodulate the data from the subcarrier, (2) bit synchronize and matched-filter detect the data, and (3) frame synchronize the data. Table 4.11 lists the principal PSP telemetry signal processing capabilities.

Commands are handled in such a manner as to (1) accept command messages in "burst" form and buffer store, (2) perform a validation check, (3) rate convert to the appropriate bit rate and prefix with an idle pattern, and (4) biphase modulate the serial command word onto a subcarrier. Data rates and signal characteristics for the command signal generation portion of the processor are tabulated in Table 4.12.

Table 4.12. PSP Command Signal Characteristics

Parameter	Value	Units
Subcarrier Waveform	Sinusoidal	-
Subcarrier Modulation	PSK, ± 90	Degrees
Subcarrier Frequency	16	kHz
Idle Pattern	Alternating "ones" & "zeros"	
Bit Rates	$2000 \div 2^N$, $N = 0, 1, 2, \dots, 8$	bps

Table 4.11. PSP Telemetry Signal Processing Capabilities

Parameter	Value	Units
Subcarrier Waveform	Sinusoidal	-
Subcarrier Modulation	PSK, ± 90	Degrees
Subcarrier Frequency	1.024	MHz
Bit Rates	16×2^N , $N = 0, 1, 2, 3, 4,$	kbps
Bit Format	NRZ-L, M, or S, or Manchester-L, M, or S	-
Word Length	8	Bits
Minor Frame Length	8 to 1024	Words
Master Frame Length	1 to 256	Minor Frames
Transition Density	≥ 64 transitions in 512 bits ≤ 64 consecutive bits w/o transition	

A functional block diagram of the PSP appears as Figure 4.10 and the ensuing paragraphs provide a description of each of the principal blocks/functions.

Telemetry signal input may be derived from either the Payload Interrogator (PI) which represents the operational input, or ground support equipment (GSE) for preflight test purposes. As the input signal is a biphas-modulated suppressed subcarrier waveform, the PSK demodulator functions to regenerate a coherent subcarrier reference which is used to phase demodulate the data from the subcarrier. Thus, the output from the PSK demodulator is the telemetry bits. Subcarrier regeneration and tracking is accomplished by means of a polarity-type Costas loop, details of which are found under subsection 4.2.2.

The bit synchronizer is a digital data transition tracking loop (DTTL) of proven design and performance. Data detection itself is performed by integrating across an entire bit (in-phase integration or averaging) and taking the resulting polarity as representative of the bit value (+1 or -1). Bit clock synchronization is accomplished by means of integrating between bits (mid-phase integration or averaging) and using the resulting measure as an error signal which subsequently corrects the local bit timing clock source phase to maintain proper alignment with the received bits. Details of the bit synchronizer are provided in subsection 4.2.3.

At the output of the bit synchronizer, a received serial telemetry data bit stream exists and is identical to that generated by the payload, with the exception of occasional bit errors. This data stream consists of random (insofar as processing is concerned) telemetry information, plus regularly inserted frame synchronization words. It is these frame synchronization words that the frame synchronization processor searches for and locks onto so that the telemetry stream output by the PSP is frame synchronized.

PSP control/mode information and command data are transferred to the PSP from the general-purpose computer (GPC) via the MDM interface. For this purpose, a serial bilateral data bus operating at a rate of 1 Mbps is employed. Also, over this same serial bus, the PSP is able to transmit a status message to the GPC for the purpose of configuration and

command data validation. Input/output in the proper mode is established to the PSP from the MDM using discrete (one-bit message) lines.

Within the PSP, a 1 MHz serial data interface is provided which performs data word detection and synchronization. All timing is generated from a master 12 MHz clock. The word validation logic examines the serial interface output to (1) check the integrity of the Manchester data waveform, (2) check parity, and (3) look for end-of-data identification. Failure to pass any of these tests results in inhibiting the Manchester-to-NRZ conversion operation.

All word valid Manchester data is converted to serial NRZ-L data, after which it is clocked into the dual buffer. The dual buffer consists of two storage memories: one which receives current data at the 1 Mbps rate, while the other is clocked out at a rate proportional to the 1.024 MHz clock. Thus, new command messages from the GPC/MDM may be received and stored at the 1 Mbps rate while, at the same time, command data may be transferred to the command subcarrier modulator at the selected payload command bit rate.

The message valid logic examines all messages received from the GPC/MDM for illegal codes. Any illegal form detected is sufficient to inhibit further processing operations. A failure to pass message validation is transmitted through the status message generator back to the GPC and a message repeat is requested.

The portion of the GPC message which corresponds to the PSP configuration information is processed by the configuration control which, in turn, is responsible for setting the PSP mode/operating parameters. Configuration status is transmitted back to the GPC via the status message generator. Command message verification is also made using status message reportback to the GPC.

Valid command bits to be transmitted to the payload are clocked from the command buffer at the proper bit rate. Each command is prefixed with a command idle pattern of alternating "ones" and "zeros". (In fact, the command idle pattern can be transmitted any time when requested and in lieu of actual command bits.) Command bits or idle pattern bits biphase modulate a 16 kHz sinusoidal subcarrier which is output to the PI.

Overall, the PSP, in Axiomatix's opinion, is well-designed and embodies up-to-date implementations. A good portion, both electrically and mechanically, is patterned after the Network Signal Processor (NSP) which has successfully completed qualification testing. Nowhere in the PSP circuits or performance measurements has Axiomatix found significant weaknesses. Therefore, the ensuing discussions will not be extensive, and will touch on only some of the more salient design details.

4.2.2 Subcarrier Demodulator

In some respects, it is useful to show the subcarrier demodulator and bit synchronizer as integral units since they function together to produce the detected telemetry bits from a noisy input signal. Figure 4.11 shows the combined block diagrams. Basically, the subcarrier demodulator and tracker are implemented using analog circuits while the bit synchronizer, on the other hand, is mechanized in a sampled data fashion using a microprocessor programmed algorithm. The analog-to-digital interface is comprised of a three-bit A/D converter (two bits magnitude plus sign). ADC sampling rate is 1.024 MHz for an analog input process whose 3 dB frequency is 250 kHz and rolls off at a rate of 12 dB/octave.

Figure 4.12 is a functional circuit diagram of the subcarrier demodulator. The input BPF is a six-pole LC T-section design which has a 3 dB bandwidth of 550 kHz. This would seem a bit more elaborate than is necessary as its only real function is to attenuate the input noise spectrum above, say, 1.25 MHz, so that no significant contribution from this region is made due to frequency translation by the odd harmonics of the following phase detector references. The phase detectors themselves are double-balanced transformer-driven diode-ring mixers (WJ-M9BC). Following each mixer is a selectable bandwidth single-pole lowpass filter. A somewhat curious aspect of the design is that TRW chose to switch the capacitor rather than the resistor to change the bandwidth. Presumably, this is done to maintain the resistive load to the mixer constant. However, it should also be noted that the mixer load is 1.16 k Ω rather than the usual 50 Ω load--this probably to minimize mixer conversion loss. Another interesting observation is that TRW specifies 1% tolerances for the arm filter capacitors. Since the actual 3 dB bandwidth of the arm filters is not critical to the noise performance of the tracking loop as

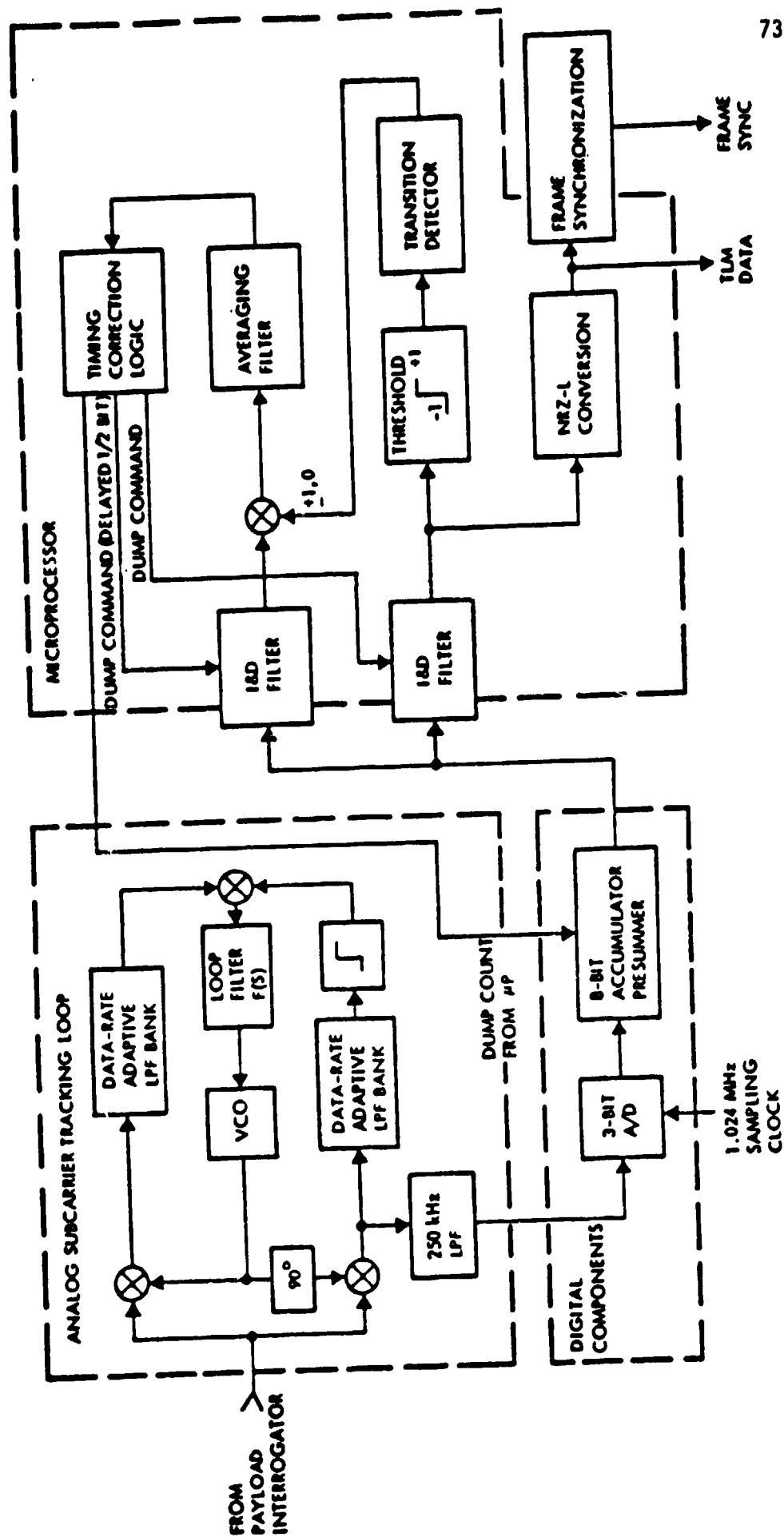


Figure 4.11. Combined Diagram for the PSP Subcarrier Demodulator and Bit Synchronizer

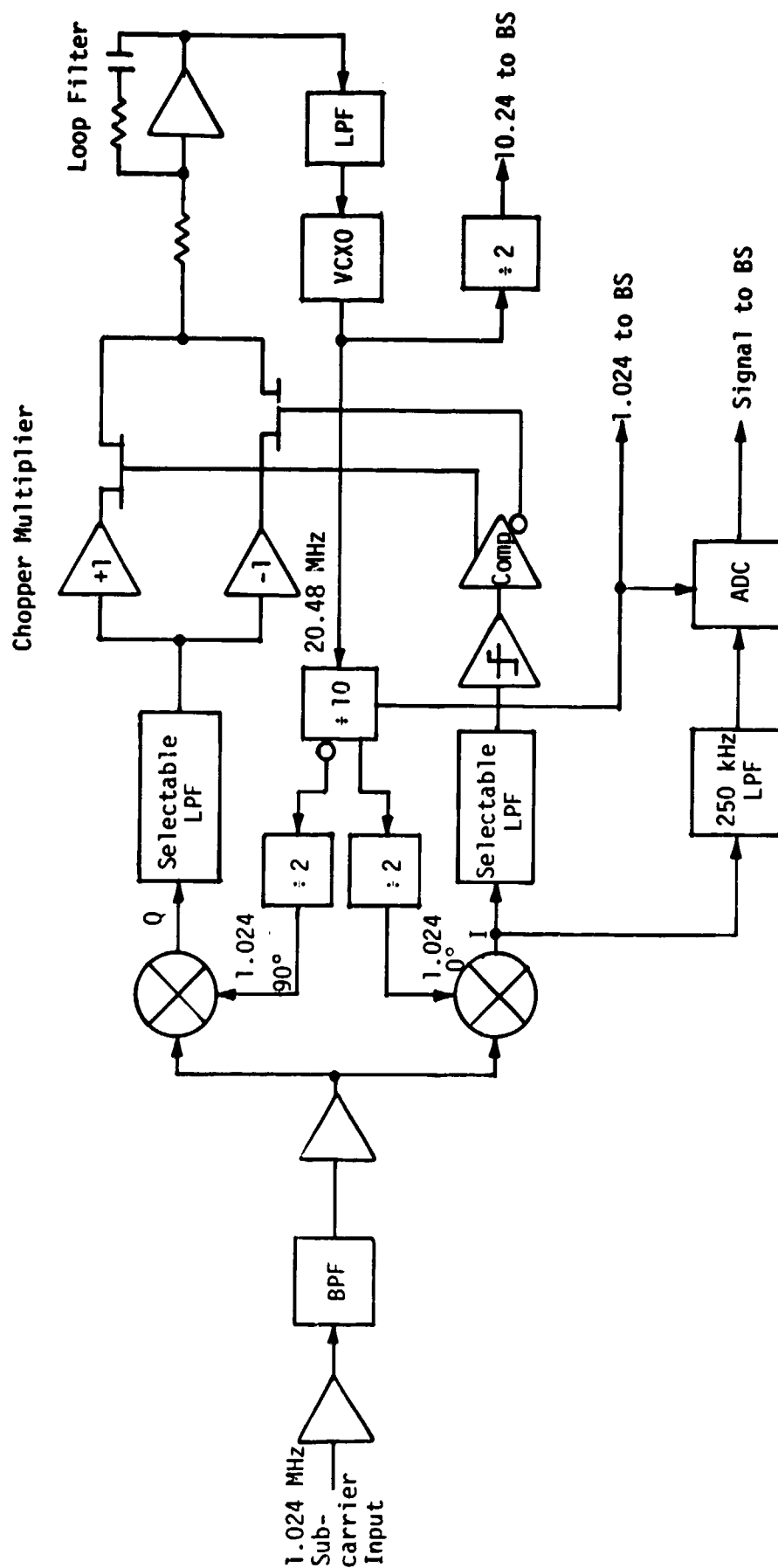


Figure 4.12. Subcarrier Demodulator Functional Circuit Diagram

long as the bandwidth is on the order of twice the data bit rate, the requirement for such accuracy is not apparent.

Following the lowpass arm filters is a chopper multiplier assembly which essentially "multiplies" together the outputs from the two arm filters. It is this product that forms the Costas loop error signal. Use of a chopper multiplier, with the switching or two-state signal being derived from the I-LPF output by means of a hard limiter, has been found, through experience, to produce good loop performance and little problem from direct voltage offsets (as is often a big problem with analog multipliers). The limiter consists of a high-gain operational amplifier followed by a comparator (LM161) which produces a pair of complementary logic waveforms at its outputs. The chopper itself is mechanized in the form of operational complementary drivers whose outputs are alternately switched, using FET switches operated by the limiter complementary waveforms, into the loop filter.

An operational type of loop filter is employed whose zero frequency gain is equal to the operational amplifier open-loop gain. (See remarks under subsection 4.1.6.) The LPF following the loop filter functions to attenuate high-frequency components, caused by the data modulation on the subcarrier, so that they cannot modulate the VCO. The VCO and the frequency dividing logic which follows it are comprised of standard, well-known, circuit configurations. One note is that the VCO is clamped so that it cannot be driven more than ± 100 Hz from its nominal frequency (20.48 MHz).

Demodulated data is recovered from the I mixer or phase detector and transferred through a two-pole LPF to the three-bit ADC. TKW selected the three-bit quantizer based upon analytical examinations of expected data SNR losses and the dynamic range of the input signal as a function of SNR and data rate. Clearly, the fewer bits for the ADC, the smaller the processor (in terms of effective register sizes) that follows. Axiomatix concurs with TRW's choice. The only qualifying comment is that the sampling rate appears unnecessarily high. At the largest data rate of 16 kbps, a 1.024 MHz sampling frequency produces 64 samples per bit. Other programs and implementations of a similar nature have shown that 16 samples per bit is sufficient and that the 0.1-0.2 dB performance gain attained by the higher sampling rate is not worth the cost (especially when it is considered that the PSP performance margin is about 0.7 dB).

TRW selected the Costas loop tracking bandwidth of $2B_L = 100$ Hz (minimum) based upon the maximum frequency uncertainty of the received subcarrier and the local VCO. The design bandwidth is about 150 Hz to allow for tolerances and aging. Analysis and testing by TRW has established that a loop minimum SNR of 10.5 dB is required to meet the sub-carrier acquisition and tracking requirements. Since this value is needed independent of data rate, the minimum E_b/N_0 that may be accommodated is a function of data rate. Table 4.13 shows the minimum E_b/N_0 for each data rate.

Table 4.13. Minimum PSP E_b/N_0 Needed to Meet Costas Loop Acquisition and Tracking Requirements

Data Rate	Acquisition E_b/N_0	Tracking E_b/N_0
1 kbps	9 dB	8 dB
2 kbps	7 dB	7 dB
4 kbps	5 dB	5 dB
3 kbps	3 dB	3 dB
10 kbps	3 dB	2 dB

4.2.3 Bit Synchronizer and Frame Sync Detector

A microprocessor is utilized to implement nearly all of the bit synchronizer functions portions of the frame synchronization algorithm. Figure 4.13 shows the functional embodiment of the bit synchronizer operating in the NRZ data mode. The microprocessor external presuming operations are necessary in that the clock rates are too fast to be accommodated within the microprocessor. Basically, the presums represent integrations (ADC samples sums) over quarter-bit periods. Thus, at the 16 kbps data rate, they are sums taken over 16 three-bit samples. The presums are then added in pairs (as indicated in Figure 4.13) to obtain half-bit integrals which are input to the microprocessor.

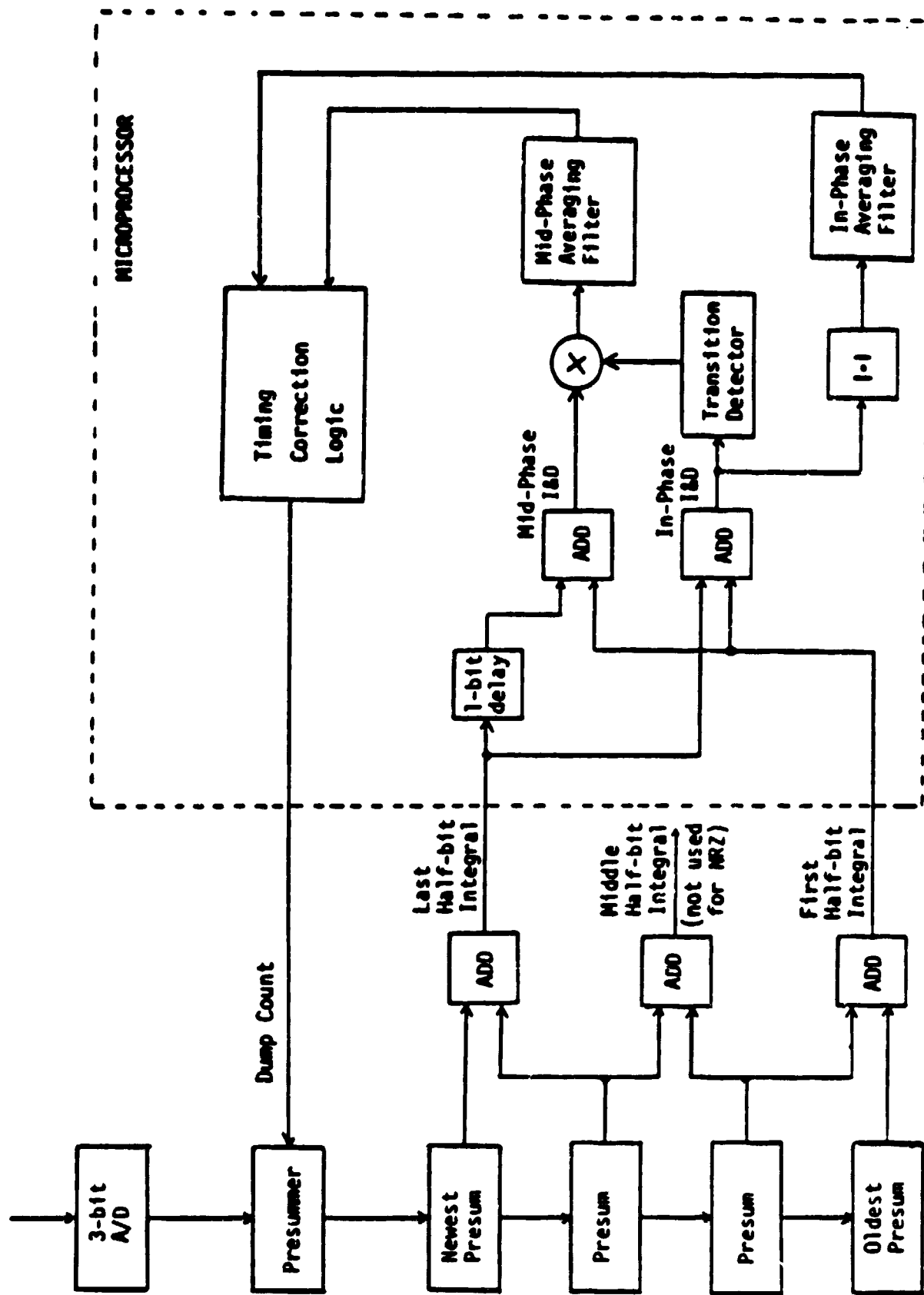


Figure 4.13. PSP Data Transition Tracking Loop for NRZ Data

The microprocessor operates to calculate the quantities needed to form the digital data transition tracking loop (DTTL) algorithm. Principal functions include in-phase and mid-phase integrate-and-dumps, a transition detector, and a clock phase advance/retard capability. This latter operation adjusts the epoch of the presum process. Data detection is obtained by extracting the sign of the in-phase integrator.

The microprocessor is an eight-bit machine developed by TRW. As TRW has done a commendable job of documenting the algorithm and program in the PSP PDR Data Package, Vol. I, further explanation and comment is unnecessary here. Additionally, the telemetry frame sync algorithm is both standard and straightforward, and no special problems exist with respect to its performance.

Prior to breadboard implementation, the PSP bit synchronizer functions were simulated and tested using a general-purpose digital computer. Breadboard measurements were subsequently performed with regard to acquisition and bit error probability (BEP). Table 4.14 summarizes typical NRZ acquisition performance, and Table 4.15 lists the BEP deviations from theoretical as measured in $\Delta E_b/N_0$ (dB).

4.2.4 Data Processing

The command data processor is a very complex algorithm that performs the major functions outlined under subsection 4.2.1. It is mechanized by means of hardwired logic. Because of its extensive nature and the fact that no major design deficiencies have been uncovered, a further explanation of its operation will not be presented in this report. The interested reader is referred to the PSP PDR Data Package, Vol. I, Sections 3.1.5 and 4.1.5.

4.2.5 Command Modulator

A feature of the 16 kHz subcarrier biphase command modulator is that the entire modulated waveform is synthesized by means of a sampled data method. Figure 4.14 shows the functional configuration. A linear up/down counter is used to produce sample values of a triangular wave of frequency 16 kHz. Thus, the 1.024 MHz clock is effectively divided by 64, or there are 64 samples per cycle. Whenever the command bit reverses polarity, the direction of the count is reversed at a point

Table 4.14. Bit Synchronization NRZ Acquisition Performance

E_b/N_0 (dB)	Data Rate (kbps)	Mean Bits To Acquire	STD Bits To Acquire	No. Bits for 90% Lock Prob.
2	16	212	90	272
4	16	180	48	237
6	16	160	33	199
10	16	144	19	164
2	1	217	92	379
4	1	173	37	216
6	1	165	33	208
10	1	153	20	178

0.1% Data Rate Uncertainty
50% Transition Density

Table 4.15. Bit Synchronizer Measured BER Degradations

Data Rate	$\Delta E_b/N_0$ (NRZ-L)--dB					$\Delta E_b/N_0$ (Manchester)--dB				
	3	5	7	9	E_b/N_0 -dB	3	5	7	9	
	1k	-0.50	-0.43	-0.55	+0.32		-0.59	-0.77	-0.22	-0.22
	2k	-0.56	-0.30	+0.03	+0.45		-0.56	-0.45	-0.55	-0.24
	4k	-0.20	-0.20	-0.02	+0.13		-0.48	-0.40	-0.44	-0.37
	8k	-0.31	-0.23	-0.33	-0.42		-0.49	-0.51	-0.46	-0.57
	16k	-0.35	-0.34	-0.51	-0.89		-0.47	-0.47	-0.40	-0.60

0.00% Data Rate Uncertainty

50% NRZ-L Transition Density

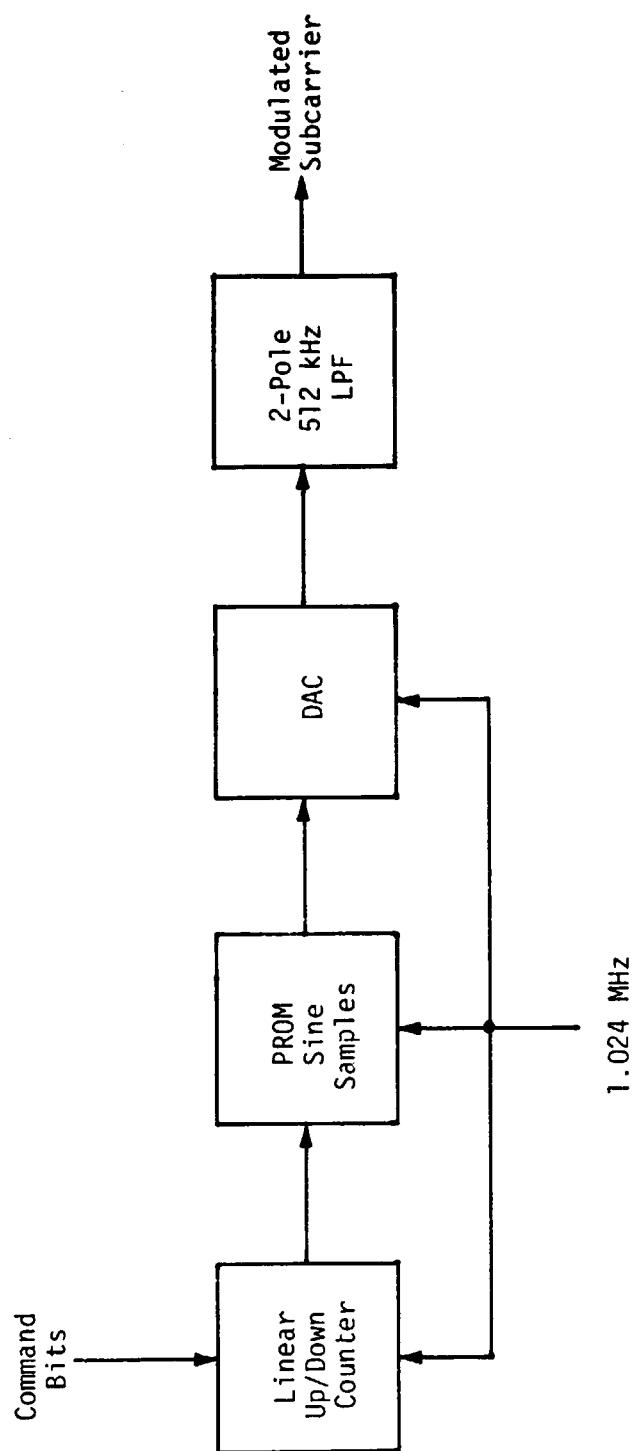


Figure 4.14. Command Biphase Subcarrier Generator

corresponding to the next triangular wave zero-crossing. For example, if the counter is increasing its count, when it reaches the value corresponding to the zero-crossing (a designated number), the counter is changed to the decreasing mode so that the count begins to decrease (rather than continuing to increase, had the command bit polarity remained unchanged). This, in effect, causes biphase modulation of the triangular wave.

The triangular wave sample values are used as sequential address locations for numbers stored in the PROM. These numbers represent sample values of a 16 kHz sinewave. Therefore, the output of the DAC is a series of pulses whose amplitudes synthesize in a stepwise fashion a sinewave with 64 steps per sample. Since the addressing triangular wave samples are biphase modulated, so is the resulting sinewave.

A two-pole lowpass filter with a 3 dB frequency of 512 kHz is used to smooth the step-approximated sinewave. Its output thus becomes a nearly pure biphase modulated sinewave (harmonic content = 0.2%), with a nominal frequency (16 kHz) accuracy of +0.001%.

4.3 Network Transponder QTP Evaluations

4.3.1 Task Plan

The purpose of this report is to summarize the findings after reviewing the TRW S-band network transponder qualification test procedure (QTP) WR-06Q-04, Rev. A2. This report is the result of a very extensive review of the TRW QTP and meets the task objectives.

The objective of the TRW network transponder QTP review was to examine the test procedure in detail. To be included was an assessment of the following items:

- (1) Nature of the tests
- (2) Appropriateness of the tests
- (3) Inconsistencies
- (4) Omissions
- (5) Usefulness of the test data
- (6) Test procedures, equipment and methods.

4.3.2 Approach

The review was divided into two phases. The first phase addressed the overall TRW QTP test philosophy. Phase I examined the major test items such as thermal cycle, vibration and life tests.

The second phase addressed the individual TRW tests to determine whether the test satisfied the applicable paragraphs of the Rockwell International (RI) specification. Phase II examined the detailed test items such as acquisition, bit error rate and RF power output tests. In both phases, the baseline document was RI Specification MC 478-0106, Rev. E, Seq. 04.

During the first or major test item review phase, some omissions and inconsistencies were discovered. For the second or detailed test item review phase, a test matrix was constructed to help uncover omissions and inconsistencies and determine the appropriateness of the tests. This test matrix also indicated some omissions and inconsistencies. Many of these apparent omissions and inconsistencies are being addressed or have been explained by the appropriate RI personnel.

4.3.3 QTP Description

The objective of any QTP is to qualify the equipment design whereas the acceptance test procedure (ATP) objective is to verify that the equipment has been correctly manufactured. A proper QTP, therefore, will test equipment at specification limits to uncover design deficiencies.

The purpose of TRW QTP WR-06Q-04, Rev A2, is to ensure that the S-band network transponder design meets Rockwell International (RI) equipment specification MC 478-0106, Rev E, Seq. 04 and, for the most part, the QTP tests the transponder at the specification limits. Once qualification testing is concluded, subsequent transponders are accepted upon completion of the less rigorous ATP. Qualification testing, therefore, is vital in assuring that the transponder will meet its mission requirements.

The two-volume TRW network transponder QTP consists of the RI-specified tests shown in Table 4.16. The first full functional test shown in this table provides the baseline data for comparing the transponder performance before and after the qualification test. During each test, selected functional tests are conducted to verify that the unit is meeting the performance requirements. At the end of most tests (such as thermal cycle and vibration), a limited functional test confirms that the transponder has not been degraded from the previous test. In the event of a failure, the limited functional test serves to isolate the test phase during which the failure occurred. For additional details, Table 4.17 lists the objectives of each test shown in Table 4.16.

Table 4.16. Test Sequence

1. Full Functional Test	7. Thermal Vacuum Test
2. Power Test	8. Limited Functional Test
3. Thermal Cycle Test	9. Life Test
4. Limited Functional Test	10. Shock Test
5. Vibration Test	11. Full Functional Test
6. Limited Functional Test	12. Leakage Test
13. EMC Test	

Table 4.17. Test Purposes

1. Full Functional Test

Provides baseline comparative data.

2. Power Test

Selected functional tests are performed to assure that the transponder meets all performance requirements including power consumption under high and low primary input power conditions.

3. Thermal Cycle Test

The unit is cycled limit-to-limit 10 times and selected functional tests are conducted at high and low temperature extremes to verify acceptable performance.

4. Limited Functional Test

This test verifies the postthermal cycle transponder performance.

5. Vibration

The unit is subjected to two different vibration tests in each of three orthogonal axes--qualification acceptance vibration test (QAVT) and flight vibration test. Selected functional tests are performed during both vibration tests.

6. Limited Functional Test

This test verifies postvibration transponder performance.

7. Thermal Vacuum Test

Selected functional tests are conducted to assure that the transponder meets all performance requirements in a low-pressure, constant-temperature environment.

8. Limited Functional Test

This test verifies postthermal vacuum transponder performance.

9. Life Test

The transponder is subjected to a given number of on/off cycles in each prime mode of SGLS, STDN and TDRS, followed by a selected functional test.

Table 4.17. Test Purposes (Cont'd)

10. Shock Test

With the unit off, the transponder is shock-tested in each of three orthogonal axes (both directions)

11. Full Functional Test

By comparing this test with the first functional test results, any performance degradation is detected.

12. Leakage Test

Since the unit is pressurized internally, the leak rate must be verified.

13. EMC Test

This test determines the electromagnetic compatibility of the transponder.

4.3.4 QTP Assessment

Overall, TRW is very adequately meeting the intent of the RI specification, however, some questions need to be resolved. There are some significant questions concerning the test procedures and test methods used for verifying the transponder performance as well as some questions relating to the QTP documentation itself.

The documentation questions are included in this report because the QTP contains baseline data that will be required in the future. Any potential confusion or inconsistencies will hinder personnel in using the data or the test procedure.

The QTP assessment is divided into three sections. The first one discusses questions dealing with the major QTP tests, the second discusses questions dealing with the detailed QTP tests, and the third discusses questions dealing with RI specification paragraphs not tested during the TRW QTP.

4.3.4.1 TRW major QTP test items assessment

This section discusses those questions dealing with the major test items such as thermal cycle and vibration tests. (Reference Table 4.18 for summary.)

Each major test item was reviewed in detail and compared against the RI requirements. Also, each major test item was reviewed from the viewpoint of an independent observer.

Since the network transponder is very complicated, some judgments had to be exercised by RI and TRW as to how to adequately test the unit in a reasonable time frame. The judgments exercised by RI and TRW appear to be adequate to ensure proper testing. Five observations made during this phase of the QTP assessment are described in detail below.

4.3.4.1.1 Paragraph 1.3, Test Description, Vol. I, Page 1

This comment concerns the QTP documentation. The test sequence outlined in Table I of the QTP is slightly different than the sequence outlined in the RI specification. TRW tests EMC following the shock test, yet RI specifies EMC following the power test. The purpose for mentioning the difference in sequences is to avoid any future quality assurance and inspection problems.

Table 4.18. S-Band Network Transponder
TRW Major QTP Tests from WR-06Q-04 Rev A2

Item No.	TRW QTP Paragraph	Comments	Resolution
1.	1.3	TRW tests EMC following shock test, yet RI specifies EMC following power test.	
2.	2.3	TRW document WR-06H-20 is required for test 3.3.14, BER, but this document isn't listed in Paragraph 2.3, <u>Applicable Documents</u> .	
3.	3.7	RI specifies that the unit be cycled between two temperature extremes of +120°F air and -20°F air but allows the functional tests to be performed at +95°F and +45°F.	RI states that the +95°F air and +45°F air are the absolute worst-case temperatures that the unit will experience. Further investigation is warranted to determine if adequate margins exist.
4.	3.9	RI requires specific specification paragraphs to be tested during vibration; however, TRW included only some of the detailed QTP tests to test these paragraphs and eliminated others. The most apparent reason for this is the limited amount of time available to conduct tests during vibration.	Many of the items are indirectly tested since all telemetry, input power and transmitter output power are continuously monitored by strip chart. The only concern is that there is no specific QTP paragraph that requires strip charts to be reviewed.
5.	3.9	Confusing nomenclature, "phase noise," used instead of "carrier phase stability."	

4.3.4.1.2 Paragraph 2.3, Applicable Documents, Vol. I, Page 2

For the BER tests (TRW Test 3.3-14), TRW document WR-06H-20 is referred to in QTP Vol. I, pp 68, 78, 131 and 168, and in QTP Vol. II, pp 115 and 157. This document is not listed in Paragraph 2-3, Applicable Documents, however.

4.3.4.1.3 Paragraph 3.7, Thermal Cycle Test--General, Vol. I, Page 9

The thermal cycle test consists of 5.5 cycles from +120°F air (+122°F baseplate) to -20°F air (+37°F baseplate), with major functional tests at the end of the 5.5 cycles. The major functional tests are conducted at +95°F air (+112°F baseplate) and +45°F air (+72°F baseplate).

RI states that +95°F and +45°F represent the absolute worst-case temperature extremes that the transponder will experience in actual operation. If there is a possibility that the transponder will ever experience these temperature extremes, it would be prudent for qualification to require the unit to function at higher and lower temperatures than those presently specified.

4.3.4.1.4 Paragraph 3.9, Vibration, Vol. I, Page 20

RI specifies that a number of tests be performed during vibration yet, in Table 8, QAVT Vibration Test Matrix, Vol. I, p 26, and in Table 9, Flight Vibration Test Matrix, Vol. I, pp 27 and 28, TRW performs only some of these tests. Because of the relatively short time available for qualification and flight vibration and the relatively long time required to perform the RI-specified tests, it seems that TRW made a reasonable choice of tests to fit into the time allotted for vibration.

TRW uses very specific and detailed tests to verify power consumption, loop stress telemetry, AGC, transmitter output power stability and the transmitter output power monitor. TRW eliminated these specific tests; however, many of these items are tested indirectly since all telemetry, input power and transmitter output power are monitored continuously on a strip chart recorder. The only concern is that there is no specific paragraph in the QTP requiring that the strip charts be reviewed for out-of-specification conditions.

4.3.4.1.5 Paragraph 3.9, Vibration, Vol. I, Page 20

This comment concerns nomenclature which might cause confusion. Using the term "phase noise" in four places to describe TRW Test 3.3.18 seems confusing since all the appropriate data sheets in the QTP and the ATP use the term "carrier phase stability." "Phase noise" is used in Table 8, Vol. I, p 26, items 1-4; Table 9, Vol. I, p 27, items 1-4; paragraph 3.9.4.1, Vol. I, p 29; and paragraph 3.9.5.1, Vol. I, p 31.

4.3.4.2 TRW detailed QTP test assessment

This section discusses those questions dealing with the detailed test items such as acquisition, bit error rate and RF output power tests. (Reference Table 4.19 for summary.)

Each detailed test was reviewed and compared against the RI requirements. The detailed tests appear very adequate and only six observations were made, as described below.

4.3.4.2.1 Test 3.3.1, Power Consumption Test

This comment concerns documentation. In Configuration 1, the input frequency should be 1775.733 MHz, not 1775.773 MHz (probable typo). Test 3.3.1 data sheets are in Vol. I, pp 43, 44, 111, 148 and 185, and in Vol. II, pp 65 and 134.

4.3.4.2.2 Test 3.3.3, Operational Modes Test

This is another documentation comment. In Configuration 7, the input level should be -70 dBm--not -80 dBm (probable typo). Test 3.3.3 data sheets are in Vol. I, pp 47, 113 and 150, and Vol. II, pp 65 and 134.

4.3.4.2.3 Test 3.3.9.3, Acquisition Time and Carrier False Lock

This test allows an acceptable acquisition time of ≤ 12 seconds for all four primary modes. Twelve (12) seconds applies only to the TDRS mode and ≤ 6 seconds should be specified for SGLS, STDN and STDN Hi-Power modes, as per the RI specification. Test 3.3.9.3 data sheets are in Vol. I, pp 48-51, 117-118, 154-155, 188-189, and Vol. II, pp 46-47, 66-67, 82-83, 106-107, and 140-141.

Table 4.19. S-Band Network Transponder
TRW Detailed QTP Tests From WR-06Q-04, Rev. A2

Item No.	TRW Test Number	Comments	Resolution
1.	3.3.1	Typo--Configuration 1. Should be 1775.733--not 1775.773 MHz.	
2.	3.3.3	Typo--Configuration 7. Should be -70 dBm--not -80 dBm.	
3.	3.3.9.3	Specifies acceptable acquisition time of ≤ 12 seconds for all four primary modes. This 12 seconds applies only to TDRS; ≤ 6 seconds S/B specified for SGLS, STDN and STDN Hi-Power.	
4.	3.3.14	<p>(1) TRW should verify proper operation within the RI-specified BER range sometime during qualification. Vibration or temperature would be a good test indicator.</p> <p>(2) The test points used to verify STDN Hi-Power, high data rate with ranging, are out of spec.</p> <p>(3) The TDRS BER tests are inadequate.</p>	
5.	3.3.21	Pass limit indicated S/B ≤ 2.0 dB, not ≤ 1.0 dB for TDRS.	
6.	3.3.14 and 3.3.22	This review did not verify that test equipment switch position changes listed for each test were correct; however, there is suspicion that the switch position changes required by the test operator were not listed for test 3.3.14, configurations 13 and 15, and for test 3.3.22.	

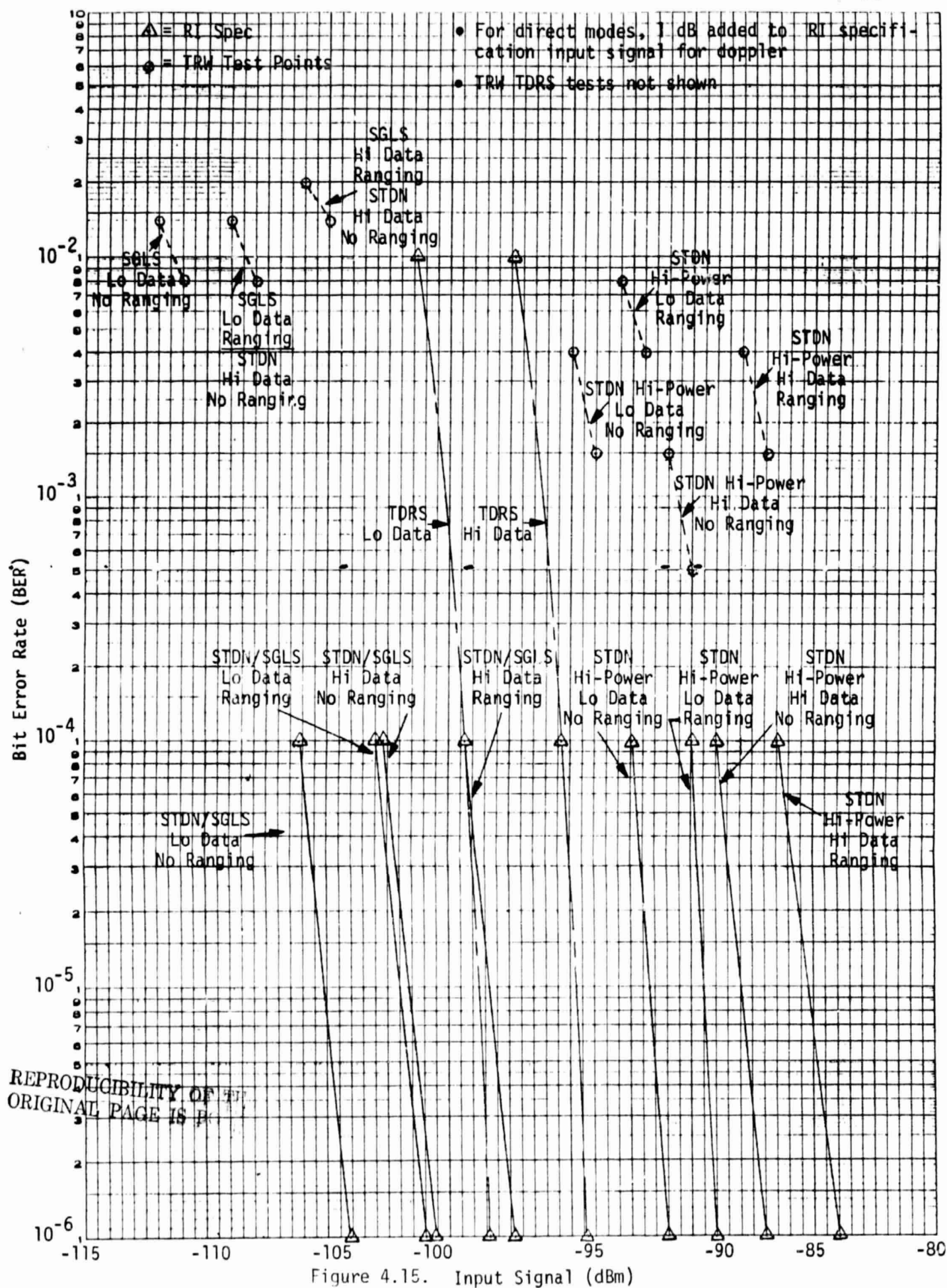
4.3.4.2.4 Test 3.3.1.14, BER

There are three comments concerning the bit error rate tests. The first comment concerns the test points which TRW selected to verify compliance with the BER requirements. Figure 4.15 illustrates both the RI specification BER versus input signal and the TRW test points. TRW conducts extensive BER tests but, as Figure 4.15 indicates, TRW is testing at points higher on the BER curve than the range which the RI specification covers. The comment is that, at least sometime during the QTP, proper operation within the RI specification range should be verified. There is no issue that TRW is testing at points higher on the BER curve than the range of the RI specification. This is reasonable since performing all of the BER tests within the RI specification range would require extremely long time periods. For example, to verify error rates of 10^{-6} , a sample of at least 10^8 counts would be required to perform the test. Besides requiring long time periods to perform the BER tests at 10^{-6} , keeping test conditions constant of 52.1 minutes is difficult. The issue is that, even though the transponder performs adequately at points higher on the BER curve, anomalies may still occur at the lower BER levels.

One good test indicator would be to verify the BER within the RI specification range during vibration since vibration tends to introduce phase instabilities. Another good test indicator would be to verify the BER within the RI specification range over temperature.

The second comment concerns an out-of-specification condition. By extrapolating the RI BER curve, it appears that TRW tests at input signal levels that adequately meet the RI BER specification for all direct modes. However, for the case of STDN high power, high data rate with ranging, the TRW test points are outside the extrapolated RI curve.

The third comment concerns the TDRS BER tests which appear inadequate. For the nonspread spectrum, uncoded transponder modes of SGLS, STDN and STDN HI-POWER, the BER qualification tests are straightforward. The transponder receives data at a given RF power level and rate, and the data is sampled for a given number of counts. During the sampling time, the input data is compared with the output data to determine the number of bit errors. Finally, the number of errors is compared to the pass/fail criteria.



The BER tests for the TDRS mode become somewhat complicated because the TDRS mode employs convolutional encoding. One method that can be used to verify the TDRS BER performance is to monitor the data prior to encoding, encode the data, input the RF signal to the transponder at a given power level, and monitor the output of the network signal processor (NSP). This would simulate actual operating conditions. By carefully calibrating the test setup, a most representative measure of the system BER performance would be obtained. In fact, this method is as straightforward as that employed for the other three primary modes. In order to implement this testing method, however, an NSP would have to be dedicated to the acceptance and qualification tests.

TRW elected not to dedicate an NSP to the transponder acceptance and qualification tests, so they selected a second method to verify TDRS BER performance. Appendix B is TRW document WR-06H-20A, "Procedure to Calibrate the Shuttle LRU Test Set Commercial Bit Synchronization Against the EM NSP Bit Synchronization." This document, along with the transponder QTP, outlines a method to test the BER performance without a dedicated NSP.

The TRW approach is outlined as follows:

(1) The BER performance at 32 kbps coded and 32 kbps uncoded is measured using the engineering model (EM) transponder and the EM NSP.

(2) The BER performance at 32 kbps uncoded is measured using the EM transponder and a commercial bit synchronizer/detector.

(3) By comparing the uncoded results obtained with the NSP and the uncoded results obtained with the commercial bit synchronizer/detector, a calibration "delta" between the two BER curves is obtained.

(4) With the commercial unit then "calibrated" against the NSP, the input data rate is dropped from 32 to 10.29 kbps to simulate the "coded" bit rate.

(5) The 10.29 kbps bit rate was determined by TRW to be that rate at which the uncoded BER curve intercepts the 32 kbps coded BER curve at an error probability of $P_E = 10^{-4}$. Thus, TRW uses 10.29 kbps uncoded to simulate 32 kbps coded.

(6) A BER curve is generated with the results obtained at 10.29 kbps. By taking this curve and adding 0.3 dB, a pass/fail curve is generated for the EM transponder and commercial synchronizer combinations.

(7) By using the calibration "delta" and the curve obtained for 10.29 kbps, TRW states that the results are equivalent to the RI specification at an error probability of $P_E = 10^{-4}$.

(8) Subsequent transponders tested with the commercial synchronizer are now compared to the EM results at $P_E = 10^{-4}$ for a 10.29 kbps data rate; a criterion for passing is that the results fall within the EM BER pass/fail curve at $P_E = 10^{-4}$.

(9) In the QTP, TRW identifies and quantifies various sources of data degradation, such as spread spectrum code phasing error, filtering, phase noise, phase bias and phase bias shifts over temperature, as additional indicators to the transponder performance. These sources of data degradation are used as additional pass/fail criteria for both the TDRS low (32 kbps or 96 ksps) and high (72 kbps or 216 ksps) data rates as simulated by 10.29 kbps and 26.18 kbps, respectively. The 26.18 kbps is used to simulate the 72 kbps high data rate and is derived in a manner similar to that used to derive the 10.29 kbps used to simulate the 32 kbps low data rate.

There are three problems with the procedure TRW uses to verify TDRS BER performance, listed as follows:

(1) There is an underlying assumption that the calibration "delta" between the EM NSP and the commercial bit synchronizer is constant since it is measured only once. Slight changes in the test setup and time could influence this "delta."

(2) The relative BER performance of all transponders is being verified at only one point, $P_E = 10^{-4}$, and at only the low data rate of coded 32 kbps as simulated by uncoded 10.29 kbps. The BER performance is not verified at the high data rate of coded 72 kbps.

(3) The transponder bandpass characteristics are designed to accommodate the specific high data rate of 72 kbps (216 ksps), but making verifications at the simulated lower rate of 10.29 kbps does not indicate the amount of filter loss. It is possible that there could be degradation at the high data rate that would not be detected when using the simulated low rate.

The method used by TRW to verify the TDRS BER performance raises some questions as to the adequacy of the test. TRW states in the document shown in Appendix B that the method used "... is significantly poorer than that which can be obtained using the method outlined in the functional test procedure (FTP). This is why the FTP method is used for primary sell-off."

TRW is using the same method in the QTP as in the FTP to verify BER performance, but this applies only to the SGLS, STDN and STDN HI-POWER MODES. The method outlined in this report is the one used to verify TDRS BER performance. Since the TDRS test method is significantly poorer and TDRS performance is somewhat critical, it is strongly suggested that an NSP be used to verify the TDRS mode, especially at the 72 kbps data rate.

4.3.4.2.5 Test 3.3.21, Transmitter Frequency Response Test

Pass limit should be specified as ≤ 2.0 dB--not ≤ 1.0 dB for the TDRS mode. Test 3.3.21 data sheets are in Vol. I, pages 143 and 180, and Vol. II, page 170.

4.3.4.2.6 General

This comment concerns documentation. In each test data sheet, switch position changes are listed so that the operator can change test modes. While this review did not get into the detail of whether or not the switch position changes listed actually place the transponder in the required mode, there are two situations that appear suspicious. In test 3.3.14, BER, configurations 13 and 15 show no switch position appears to change modes. Also, in test 3.3.22, Loop Stress Telemetry, no switch position changes are shown.

Test 3.3.14 data sheets listing configurations 13 and 15 are in Vol. I, pp 65, 75, 128, 165 and 193, and Vol. II, pp 51, 70, 87, 112 and 154. Test 3.3.22 data sheets are in Vol. I, pp 92, 93, 114, 181 and 203, and Vol. II, pp 61, 97 and 171.

4.3.4.3 RI paragraphs not tested during QTP

This section discusses those questions dealing with the RI paragraphs not tested during the QTP. A test matrix was constructed to compare the RI specification paragraphs with the appropriate TRW detailed tests. This test matrix is shown in Table 4.20.

As the matrix indicates, TRW does not necessarily test each RI paragraph in all four primary modes. During the review, the requirements for each paragraph were compared to the test methods used and the modes tested. The conclusion is that the modes which TRW selected for testing each paragraph are comprehensively adequate.

Table 4.21 lists those 10 paragraphs which were not tested during the QTP. Some of the paragraphs are tested prior to final assembly and one paragraph (RI 10.3.2.1.2.1.3.1), dealing with RF overload protection at the common port appears to have been overlooked.

4.3.5 Recommendations

Overall, TRW is meeting the intent of the RI specification. The test methods and procedures used to perform the RI specification verifications adequately test the S-band network transponder in all the critical modes. It is recommended that all issues discussed in this report be addressed and resolved, especially the three following items:

(1) Section 4.3.4.1.3, Thermal Cycle Test.

To determine if adequate performance margins exist, the functional tests should be conducted at the specification extremes of +120°F and -20°F instead of +95°F and +45°F.

(2) Section 4.3.4.2.4, BER.

- Proper operation within the RI-specified BER range should be verified at least once
- An NSP should be used to perform the TDRS BER tests.

(3) Table 9, item 4

- Test the common port for RF overload protection.

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Table 4.20. RI Transponder Specification versus Operational Modes

Specification Paragraph (i)	Specification Title/Test Criteria (j)	SGLS Mode			STDN Mode			STDN HI-Power Mode			TDRS Mode			Paragraph Not Tested During QTP	
		Lo Freq. Data	Hi Freq. Data	Hi Freq. Data	Lo Freq. Data	Hi Freq. Data	Hi Freq. Data	Lo Freq. Data	Hi Freq. Data	Hi Freq. Data	Lo Freq. Data	Hi Freq. Data	Hi Freq. Data		
1. 10.3.1.2.1	Electrical Power Characteristics • Power Consumption @ 28 VDC	1	*	*	*	1	*	*	1	*	*	*	1		
2. 10.3.1.2.4.1.1.1	Displys & Cnls Interface/Input Signals	24	24	24	24	24	24	24	24	24	24	24	24		
3. 10.3.1.2.4.1.2.1	Ant. Sw. Assy Interface/Input Signals	X	X	X	X	X	X	X	X	X	X	X	X		
4. 10.3.1.2.4.1.2.2	Preamp Assy Interface/Input Signals	X	X	X	X	X	X	X	X	X	X	X	X		
5. 10.3.1.2.4.1.3-1.4	NSP 1/NSP 2 Interface/Ser. Digital Input	X	X	X	X	X	X	X	X	X	X	X	X		
6. 10.3.1.2.4.2.1	MDM Interface/Xpndr Output Signals	*	*	*	*	*	*	*	*	*	*	*	*		
7. 10.3.1.2.4.2.2	Doppler interface/Discr. Output	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted		
8. 10.3.1.2.4.2.3	Ant. Sw. Assy Interface/Output Signals	X	X	X	X	X	X	X	X	X	X	X	X		
9. 10.3.1.2.4.2.4	Power Amplifier Assembly	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted		
10. 10.3.1.2.4.2.5	Doppler Extractor Interface/Output	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted	Deleted		
11. 10.3.1.2.4.2.6	MDM Interface/Xpndr Output Signals • RF Power Monitor--Coherent • RF Power Monitor--Noncoherent • AGC • Loop Stress	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	16 16 11.4 22 22 22 22 22	
12. 10.3.1.2.4.2.7-2.8	NSP 1/NSP 2 Interface/Xpndr Output	11.4 22	22 22	22 22	11.4 22	22 22	22 22	11.4 22	22 22	22 22	11.4 22	22 22	11.4 22	11.4 22	
13. 10.3.1.2.4.2.9	Displays & Cntl Interface/AGC Output	*	*	*	*	*	*	*	*	*	*	*	*	*	
14. 10.3.2.1.2.1.1	Xpndr Operational Modes • Warm-up time	11.4 24	24 24	24 24	11.4 24	24 24	24 24	11.4 24	24 24	24 24	11.4 24	24 24	11.4 24	11.4 24	
15. 10.3.2.1.2.1.1.1	Mode Selection (Prime & Secondary) • Xmitr Output Disabled During Prime • Mode of Freq. Mode Switch • NSP 1/NSP 2 Xmit Data Disable • Control Current Drain	X X X X X 24	X X X X X 24	X X X X X 24	X X X X X 24	X X X X X 24	X X X X X 24	X X X X X 24	X X X X X 24	X X X X X 24	X X X X X 24	X X X X X 24	X X X X X 24	X X X X X 24	
16. 10.3.2.1.2.1.2	Doppler Orbital Tracking	4	4	4	4	4	4	4	4	4	4	4	4	4	
17. 10.3.2.1.2.1.3	RF Input/Output Characteristics • Common to TDRS Out. Iso. • TDRS Out. to Common Iso. • Common to TDRS In. Iso.	5	5	5	5	5	5	5	5	5	5	5	5	5	
18. 10.3.2.1.2.1.3.1	I/O Impedance & I/O Protection • Input Impedance • Output Impedance • Common Port RF Overload Protection • TDRS Port RF Overload Protection • Output Short/Open Protection	6 6 6 3.5-1A(3) 7.8	6 6 6 6 7.8	6 6 6 6 7.8	6 6 6 6 7.8	6 6 6 6 7.8	6 6 6 6 7.8	6 6 6 6 7.8	6 6 6 6 7.8	6 6 6 6 7.8	6 6 6 6 7.8	6 6 6 6 7.8	6 6 6 6 7.8	6 6 6 6 7.8	
19. 10.3.2.1.2.1.3.2	Tone Ranging Turnaround Capability	8	8	8	8	8	8	8	8	8	8	8	8	8	
20. 10.3.2.1.2.1.3.2.1	Tone Ranging Modulation Format	X	X	X	X	X	X	X	X	X	X	X	X	X	
21. 10.3.2.1.2.1.3.2.2	Tone Ranging Turnaround Freq. Response	7	7	7	7	7	7	7	7	7	7	7	7	7	
22. 10.3.2.1.2.1.3.2.3	Tone Ranging Turnaround Delay Time	8	8	8	8	8	8	8	8	8	8	8	8	8	
23. 10.3.2.1.2.1.3.2.4	Tone Ranging Turnaround Delay Time Var.	8	8	8	8	8	8	8	8	8	8	8	8	8	

Table 4.20. RI Transponder Specification versus Operational Modes (Cont'd)

Specification Paragraph (i)	Specification Title/Test Criteria (3)	SGLS Mode			STDN Mode			STDN HI-Power Mode			TDRS Mode			Paragraph Not Tested During QTP
		Lo Freq. Data	Hi Freq. Data	Lo Freq. Data	Lo Freq. Data	Hi Freq. Data	Lo Freq. Data	Lo Freq. Data	Hi Freq. Data	Lo Freq. Data	Lo Freq. Data	Hi Freq. Data	Lo Freq. Data	
24. 10.3.2.1.2.1.4	Receiver • Capabilities • Noise Figure • Frequency Response	X	X	X	X	X	X	X	X	X	X	X	X	
25. 10.3.2.1.2.1.4.1	RF Input Characteristics	X	X	X	X	X	X	X	X	X	X	X	X	
26. 10.3.2.1.2.1.4.1.1	Input Frequency	X	X	X	X	X	X	X	X	X	X	X	X	
27. 10.3.2.1.2.1.4.1.2	Doppler Freq. Shift and Rate • Shift • Rate (°)	X	X	X	X	X	X	X	X	X	X	X	X	
28. 10.3.2.1.2.1.4.1.3	Acquisition	X	X	X	X	X	X	X	X	X	X	X	X	
29. 10.3.2.1.2.1.4.1.3.1	Acquisition Sweep	X	X	X	X	X	X	X	X	X	X	X	X	
30. 10.3.2.1.2.1.4.1.3.2	Acquisition Threshold	X	X	X	X	X	X	X	X	X	X	X	X	
31. 10.3.2.1.2.1.4.1.3.3	In-Lock Tracking (1)	X	X	X	X	X	X	X	X	X	X	X	X	
32. 10.3.2.1.2.1.4.1.3.4	Tracking Threshold	X	X	X	X	X	X	X	X	X	X	X	X	
33. 10.3.2.1.2.1.4.1.3.5	Tracking Phase Error	X	X	X	X	X	X	X	X	X	X	X	X	
34. 10.3.2.1.2.1.4.1.3.6	Tracking Loop Stress TLM Measurement	X	X	X	X	X	X	X	X	X	X	X	X	
35. 10.3.2.1.2.1.4.1.4	Received Signal Transients	X	X	X	X	X	X	X	X	X	X	X	X	
36. 10.3.2.1.2.1.4.1.5	Interference Rejection	X	X	X	X	X	X	X	X	X	X	X	X	
37. 10.3.2.1.2.1.4.2	Data Demodulation	X	X	X	X	X	X	X	X	X	X	X	X	
38. 10.3.2.1.2.1.4.3	AGC • Over Receiver Dynamic Range • Response Time	X	X	X	X	X	X	X	X	X	X	X	X	
39. 10.3.2.1.2.1.4.3.1	AGC TLM Meas. Resolution & Repeat.	X	X	X	X	X	X	X	X	X	X	X	X	
40. 10.3.2.1.2.1.4.3.2	AGC Signal Strength Output	X	X	X	X	X	X	X	X	X	X	X	X	
41. 10.3.2.1.2.1.4.4	Doppler Extractor Interface	X	X	X	X	X	X	X	X	X	X	X	X	
42. 10.3.2.1.2.1.4.4.1	Prime and Frequency Mode Status	X	X	X	X	X	X	X	X	X	X	X	X	
43. 10.3.2.1.2.1.4.4.2	Doppler Data Quality Status	X	X	X	X	X	X	X	X	X	X	X	X	
44. 10.3.2.1.2.1.4.4.3	Doppler Extractor Output Signals	X	X	X	X	X	X	X	X	X	X	X	X	
45. 10.3.2.1.2.1.4.5	Recvr. Bit Error Rate Performance • BER N = 10 ⁵ , 10 ⁶ w/Dop. w/o p. ing • BER N = 10 ⁵ , 10 ⁶ w/Dop. w/o p. ing • BER N = 10 ⁵ , 10 ⁶ w/Dop. and Range • BER N = 10 ⁵ , 10 ⁶ w/Dop. and Spread. g	X	X	X	X	X	X	X	X	X	X	X	X	
46. 10.3.2.1.2.1.4.6	TDRS RF Input (46)	X	X	X	X	X	X	X	X	X	X	X	X	
47. 10.3.2.1.2.1.4.7	Spread Spectrum	X	X	X	X	X	X	X	X	X	X	X	X	
48. 10.3.2.1.2.1.4.7.1	PM Signal	X	X	X	X	X	X	X	X	X	X	X	X	
49. 10.3.2.1.2.1.4.7.2	Data Degradation	X	X	X	X	X	X	X	X	X	X	X	X	

Table 4.20. RI Transponder Specification versus Operational Modes (Cont'd)

Specification Paragraph (1)	Specification Title/Test Criteria (2)	SCLS Mode			STDM Mode			STDM HI-Power Mode			TDRS Mode			Paragraph Not Tested During QTP
		Lo Freq. Data	Hi Freq. Data	HI Data	Lo Freq. Data	Hi Freq. Data	HI Data	Lo Freq. Data	Hi Freq. Data	HI Data	Lo Freq. Data	Hi Freq. Data	HI Data	
24.	10.3.2.1.2.1.4 Receiver • Capabilities • Noise Figure • Frequency Response	X			X			X			X			
25.	10.3.2.1.2.1.4.1 RF Input Characteristics	X			X			X			X			
26.	10.3.2.1.2.1.4.1.1 Input Frequency	X			X			X			X			
27.	10.3.2.1.2.1.4.1.2 Doppler Freq. Shift and Rate • Shift • Rate (1)	X			X			X			X			
28.	10.3.2.1.2.1.4.1.3 Acquisition	X			X			X			X			
29.	10.3.2.1.2.1.4.1.3.1 Acquisition Sweep	X			X			X			X			
30.	10.3.2.1.2.1.4.1.3.2 Acquisition Threshold	X			X			X			X			
31.	10.3.2.1.2.1.4.1.3.3 In-Lock Tracking (1)	X			X			X			X			
32.	10.3.2.1.2.1.4.1.3.4 Tracking Threshold	X			X			X			X			
33.	10.3.2.1.2.1.4.1.3.5 Tracking Phase Error	X			X			X			X			
34.	10.3.2.1.2.1.4.1.3.6 Tracking Loop Stress TLM Measurement	X			X			X			X			
35.	10.3.2.1.2.1.4.1.4 Received Signal Transients	X			X			X			X			
36.	10.3.2.1.2.1.4.1.5 Interference Rejection	X			X			X			X			
37.	10.3.2.1.2.1.4.2 Data Demodulation	X			X			X			X			
38.	10.3.2.1.2.1.4.3 AGC • Over Receiver Dynamic Range • Response Time	X			X			X			X			
39.	10.3.2.1.2.1.4.3.1 AGC TLM Meas. Resolution & Repeat	X			X			X			X			
40.	10.3.2.1.2.1.4.3.2 AGC Signal Strength Output	X			X			X			X			
41.	10.3.2.1.2.1.4.4 Doppler Extractor Interface	X			X			X			X			
42.	10.3.2.1.2.1.4.4.1 Prime and Frequency Mode Status	X			X			X			X			
43.	10.3.2.1.2.1.4.4.2 Doppler Data Quality Status	X			X			X			X			
44.	10.3.2.1.2.1.4.4.3 Doppler Extractor Output Signals	X			X			X			X			
45.	10.3.2.1.2.1.4.5 Recvr. Bit Error Rate Performance • BER N = 10 ⁵ w/Doop. w/o P. ing • BER N = 10 ⁵ w/Doop. w/o P. ing • BER N = 10 ⁵ w/Doop. and Range (1) • BER N = 10 ⁵ w/Doop. and Spread (1)	X			X			X			X			
46.	10.3.2.1.2.1.4.6 TDRS RF Input (16)	X			X			X			X			
47.	10.3.2.1.2.1.4.7 Spread Spectrum	X			X			X			X			
48.	10.3.2.1.2.1.4.7.1 PM Signal	X			X			X			X			
49.	10.3.2.1.2.1.4.7.2 Data Degradation	X			X			X			X			

Table 4.20. RI Transponder Specification versus Operational Modes (Cont'd)

Specification Paragraph (1)	Specification Title/Test Criteria (3)	SGLS Mode			STDN Mode			STDN Hi-Power Mode			TDRS Mode			Paragraph Not Tested During QTP
		Lo Freq. Data	Hi Freq. Data	Hi Freq. Data	Lo Freq. Data	Hi Freq. Data	Hi Freq. Data	Lo Freq. Data	Hi Freq. Data	Hi Freq. Data	Lo Freq. Data	Hi Freq. Data	Hi Freq. Data	
50.	3.2.1.2.1.4.7.3 PI Acquisition • Acq. Time w/Doppler • Acq. Time w/o Doppler • Time to lock													
51.	10.3.2.1.2.1.4.7.4 PI Reacquisition													
52.	10.3.2.1.2.1.5 Transmitter	X	X	X	X	X	X	X	X	X	X	X	X	
53.	10.3.2.1.2.1.5.1 Transmit Frequency • Coherent Operation • Noncoherent Operation	16	16	16	16	16	16	16	16	16	16	16	16	
54.	10.3.2.1.2.1.5.1.1 Frequency Source Switching Time	16	16	16	16	16	16	16	16	16	16	16	16	
55.	10.3.2.1.2.1.5.1.2 Transmitter Coherent TLM Discrete	16	16	16	16	16	16	16	16	16	16	16	16	
56.	10.3.2.1.2.1.5.2 RF Power Output & Output Protection • RF Power Output • Power Out Disable • Output Protection (Open & Short)	16	16	16	16	16	16	16	16	16	16	16	16	
57.	10.3.2.1.2.1.5.2.1 Power Output Stability	16	16	16	16	16	16	16	16	16	16	16	16	
58.	10.3.2.1.2.1.5.2.2 Power Output Monitor	16	16	16	16	16	16	16	16	16	16	16	16	
59.	10.3.2.1.2.1.5.2.3 Output Impedance	16	16	16	16	16	16	16	16	16	16	16	16	
60.	10.3.2.1.2.1.5.2.4 Carrier Phase Stability (noise)	16	16	16	16	16	16	16	16	16	16	16	16	
61.	10.3.2.1.2.1.5.2.5 Transmitter Spurious Outputs • Coherent Operation • Noncoherent Operation	18	18	18	18	18	18	18	18	18	18	18	18	
62.	10.3.2.1.2.1.5.3 Baseband Input Signals	19	19	19	19	19	19	19	19	19	19	19	19	
63.	10.3.2.1.2.1.5.4 Modulation • With Data (Paging Disabled) • With Data and Ranging	X	X	X	X	X	X	X	X	X	X	X	X	
64.	10.3.2.1.2.1.5.4.1 Frequency Response	20	20	20	20	20	20	20	20	20	20	20	20	
65.	Input Power Range (Selected Tests) • +24 VDC • +32 VDC	21	21	21	21	21	21	21	21	21	21	21	21	

NOTES:

(1) All specification paragraphs refer to Rockwell International S-Band Network Equipment Specification MC478-0106, Rev. E, Seq. 04

Lo	Hi
Data	Data
A	A
B	B
C	C

(2) A or B = Number. The number refers to Test Number (See Note #3).
A or B = X. Item not tested in one specific test but item is verified throughout QTP
A or B = *. Item not tested in QTP

"A" = Data present
"B" = No data present
"C" = + Doppler shift
"D" = - Doppler shift

(3) Matrix numbers refer to TRM tests 3.3. unless otherwise noted

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Table 4.21. S-Band Network Transponder
RI Specification Paragraphs (From MC 478-0106, Rev. E, Seq. 4)
Not Tested During TRW QTP

Item No.	RI Specification Paragraphs	Item Not Tested During QTP	Resolution
1.	10.3.2.1.2.1.1	Warm-up time.	Engr'g model tests indicated design greatly exceeds reqm'ts.
2.	10.3.2.1.2.1.1.1	Transmitter output disabled during prime mode or freq. mode switching.	Will be done at integration of SRU's prior to QTP.
3.	10.3.2.1.2.1.1.1	NSP 1/2 transmit data disable.	Requirements to be deleted.
4.	10.3.2.1.2.1.3.1	No damage from RF overload at common port.	RI investigating.
5.	10.3.2.1.2.1.3.2	TDRS ranging requirement.	Requirements to be deleted.
6.	10.3.2.1.2.1.4	Receiver noise figure.	Measured prior to final assy.
7.	10.3.2.1.2.1.4	Receiver frequency response.	Data supplied by triplexer vendor.
8.	10.3.2.1.2.1.4.1.3.5	Tracking phase error.	No ext. test points available to make measurements. Loop stress measurement can be translated to static phase error.
9.	10.3.2.1.2.1.5.2	RF power output disable (same as #2).	Will be done at integration of SRU's prior to QTP.
10.	10.3.2.1.2.1.5.2.1	Power output stability.	No specific test, but RF output power continuously recorded on strip chart.

4.4 ESTL Network Equipment Verification Plans Evaluation

4.4.1 Task Plan

The purpose of this report is to summarize the findings to date after evaluating the network equipment verification test plans. These tests, which are performed in the NASA Lyndon B. Johnson Space Center (JSC) Electronic System Test Laboratory (ESTL), are designed to establish that the communication links between the Orbiter and ground stations are compatible and that the system performance will meet the requirements of the Shuttle program.

To implement these tests, Orbiter and S-band network equipment hardware has been obtained and installed in a representative mission configuration in the ESTL. Therefore, the communication links to be evaluated during the tests are equivalent to those which will be used during an Orbiter mission. The only significant difference is that the RF paths will be through hard-line, space-loss simulators.

The objective of the network equipment verification test plans evaluation was to examine the ESTL S-band test procedures in detail. To be included was an assessment of the following items:

- (1) Nature of the tests
- (2) Appropriateness of the tests
- (3) Inconsistencies
- (4) Omissions
- (5) Usefulness of the test data
- (6) Test procedures, equipment and methods.

4.4.2 Approach

Before discussing the approach used in reviewing the ESTL test procedures, some history of the ESTL test program is necessary. NASA Task 501, as defined by Space Shuttle Program Manager Direction No. 51, establishes the scope of the Shuttle communication and tracking systems space-to-space and space-to-ground radio frequency performance and compatibility evaluation conducted in the JSC ESTL. This evaluation is accomplished through systems verification/certification tests using Orbiter prototype and qualifiable or flight equivalent hardware as available in conjunction with other Shuttle communications and tracking elements to

evaluate basic end-to-end system compatibility and performance and to verify/certify that operational system performance meets program requirements prior to manned flight usages.

The evaluation is divided into test series, with each series involving the Orbiter hardware and equipment representative of one of the elements with which the Orbiter must communicate. Seven test series have been designated. These series are:

- (1) Orbiter (ALT configuration) - STDN and ATR direct link
- (2) Orbiter-STDN S-band direct link
- (3) Orbiter-TDRS S-band relay link
- (4) Orbiter-EVA UHF link
- (5) Orbiter-AF/SCF S-band direct link
- (6) Orbiter-TDRS Ku-band relay link
- (7) Orbiter-Payload S-band link

For each series of system verification tests, a systems development test requirements and status (TRAS) report is published in accordance with the "Space Shuttle Program, NASA Task 501, Communications and Tracking Systems Ground Testing, System Development Plan," JSC 09687, December 1975. The TRAS reports, which are reviewed and approved by the Communications and Tracking System Ground Test (CATSGT) panel, thus provide the testing criteria for systems verification.

Once the TRAS reports have been accepted, a test plan is developed which outlines the strategy with which the TRAS requirements will be accomplished. After the test plan, a set of detailed test procedures is generated which outlines the system verification test methods.

As previously mentioned, the objective of this report is to summarize the findings to date after evaluating the ESTL S-band test procedures in detail. To accomplish this objective, the appropriate S-band TRAS reports were studied and summarized. Next, the appropriate S-band test procedures were studied and summarized and, finally, the TRAS summaries and the test procedure summaries were compared to each other to determine inconsistencies and omissions.

Axiomatix has been supplied by NASA with three TRAS reports required for this evaluation which are listed as follows:

- System Development Test Requirements and Status (TRAS)
Report for STDN S-Band Direct Link, JSC 11300,
September 28, 1977

- System Development Test Requirements and Status (TRAS)
Report for TDRS S-Band Relay Link, JSC 11757,
September 26, 1979
- System Development Test Requirements and Status (TRAS)
Report for AF/SCF S-Band Direct Link, JSC 13022,
April 11, 1978.

These three TRAS reports represent the three primary S-band equipment operational modes of GSTDN, TDRS and AF/SCF (SGLS). Axiomatix has requested the three corresponding test procedures but NASA has supplied Axiomatix with only one of the required test procedures, "System Verification Test Procedures for STDN PM Direct Link," EE7-78-107, June 1978, Volumes I-IV.

The approach used in this report, therefore, is to compare the STDN TRAS report with the STDN test procedures. In order to continue further test procedure evaluations, NASA must furnish Axiomatix with the TDRS and AF/SCF test procedures.

4.2.3 Assessment To Date

The evaluation to date compares the STDN TRAS report with the STDN test procedures. In Table 4.22, the required test parameters are listed for each TRAS number, along with the equipment operational mode in which the tests are to be conducted.

Table 4.23 lists the STDN PM direct link ESTL test procedure sections, along with the TRAS number each test section professes to meet. The purpose of this table is to give the reader an overview of the ESTL STDN S-band tests and, at the same time, correlate the test procedure sections with the TRAS requirements.

Table 4.24 lists the STDN PM direct link ESTL test procedure sections, a brief test description and the operational mode in which each test is conducted. This table allows the reader to quickly determine the conditions for each test and, at the same time, highlight any "holes" in the testing program.

By comparing Tables 4.22 through 4.24, any omissions and inconsistencies are apparent. Also, by carefully studying the STDN test procedures, comments are possible concerning the nature and appropriateness of the tests, equipment and methods.

Table 4.22. Orbiter-STDN Direct PM S-Band TRAS Requirements

TRAS No.	Link	Channel to be Tested	Parameters ⁽¹⁾	Operational Modes
SD-101	PM Uplink (Forward Link)	TDM	<ul style="list-style-type: none"> ● BER 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate ● Low-Frequency Mode <ul style="list-style-type: none"> ● Selected tests
SD-102	PM Uplink (Forward Link)	Synchronization (TDM)	<ul style="list-style-type: none"> ● BER ● Synchronization Lock ● Percent data loss 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate
SD-103	PM Uplink (Forward Link)	Synchronization (TDM)	<ul style="list-style-type: none"> ● Synchronization data quality <p>SD-103 accomplished concurrently with SD-102</p>	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate
SD-104	PM Uplink (Forward Link)	Command	<ul style="list-style-type: none"> ● BER ● Message rejection rate 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate
SD-105	PM Uplink (Forward Link)	Command	<ul style="list-style-type: none"> ● Command data quality <p>SD-105 accomplished concurrently with SD-104</p>	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate

⁽¹⁾ All parameters to be tested as a function of RF total received power.

Table 4.22. Orbiter-STDN Direct PM S-Band TRAS Requirements
(Cont'd)

TRAS No.	Link	Channel to be Tested	Parameters ⁽¹⁾	Operational Modes
SD-106	PM Uplink (Forward Link)	Voice	<ul style="list-style-type: none"> ● Voice quality ● Intelligibility ● Speech-to-noise ratio ● Signal-to-noise ratio ● BER ● Percent data loss 	<ul style="list-style-type: none"> ● Selected Modes ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate
SD-107	PM Downlink (Return Link)	TDM	<ul style="list-style-type: none"> ● BER 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate ● Low-Frequency Mode <ul style="list-style-type: none"> ● Selected tests ● Additional selected tests without uplink phase lock
SD-108	PM Downlink (Return Link)	Telemetry	<ul style="list-style-type: none"> ● BER ● Synchronization lock ● Percent data loss 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate
SD-109	PM Downlink (Return Link)	Telemetry	<ul style="list-style-type: none"> ● Telemetry functional capacity SD-109 accomplished concurrently with SD-108	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate

⁽¹⁾ All parameters to be tested as a function of RF total received power.

Table 4.22. Orbiter-STDN Direct PM S-Band TRAS Requirements
(Cont'd)

TRAS No.	Link	Channel to be Tested	Parameters ⁽¹⁾	Operational Modes
SD-110	PM Downlink (Return Link)	Voice	<ul style="list-style-type: none"> ● Voice quality ● Intelligibility ● Speech-to-noise ratio ● Signal-to-noise ratio ● BER ● Percent data loss 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate
SD-111	PM Uplink and Downlink (Forward and Return Links)	Voice	<ul style="list-style-type: none"> ● Voice functional capability SD-111 uplink accomplished concurrently with SD-106, SD-111 downlink accomplished with SD-110 ● Voice quality 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate
SD-112	PM Uplink (Forward Link)	RF Carrier	<ul style="list-style-type: none"> ● RF acquisition threshold⁽²⁾ ● RF acquisition time (2) ● RF acquisition probability (2) ● Mean time to unlock⁽²⁾ ● Carrier to noise ratio ● False lock susceptibility ● Ability to switch from PSK to ranging (PM) mode 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate ● Low-Frequency Mode <ul style="list-style-type: none"> ● Selected tests ● Selected tests without uplink TDM modulation

(1) All parameters to be tested as a function of RF total received power.

(2) With doppler offsets.

Table 4.22. Orbiter-STDN Direct PM S-Band TRAS Requirements
(Cont'd)

TRAS No.	Link	Channel to be Tested	Parameters ⁽¹⁾	Operational Modes
SD-113	PM Downlink (Return Link)	RF Carrier	<ul style="list-style-type: none"> ● RF acquisition time (2) ● RF acquisition probability (2) ● RF acquisition threshold(2) ● Mean time to unlock(2) ● Carrier-to-noise ratio ● False lock susceptibility ● Reacquisition time (2) 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate ● Low-Frequency Mode <ul style="list-style-type: none"> ● Selected tests
SD-114	PM Uplink and Downlink (Forward and Return Links)	RF Carrier	<ul style="list-style-type: none"> ● RF acquisition time (2) 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate
SD-115	PM Uplink and Downlink (Forward and Return Links)	RF Carrier	<ul style="list-style-type: none"> ● RF Acquisition functional capability SD-115 accomplished concurrently with SD-114	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate without ranging ● Low data rate
SD-116	PM Uplink and Downlink (Forward and Return Links)	Ranging	<ul style="list-style-type: none"> ● Ranging 3σ error ● Subcarrier predetection S/N ● Acquisition time (2) ● Acquisition threshold ● Postdetection S/N 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate

(1) All parameters to be tested as a function of RF total received power.

(2) With doppler offsets

Table 4.22. Orbiter-STDN Direct PM S-Band TRAS Requirements
(Cont'd)

TRAS No.	Link	Channel to be Tested	Parameters ⁽¹⁾	Operational Modes
SD-117	PM Uplink and Downlink (Forward and Return Links)	Ranging	<ul style="list-style-type: none"> ● Ranging functional capability SD-117 accomplished concurrently with SD-116	<ul style="list-style-type: none"> ● High-Frequency Mode ● High data rate
SD-118	PM Uplink (Forward Link)	One-Way Doppler	<ul style="list-style-type: none"> ● Doppler accuracy 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate ● Low-Frequency Mode ● Selected tests
SD-119	PM Uplink and Downlink (Forward and Return Links)	Two-Way Doppler	<ul style="list-style-type: none"> ● Doppler accuracy 	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate ● Low-Frequency Mode ● Selected tests
SD-120	PM Uplink and Downlink (Forward and Return Links)	Doppler Tracking	<ul style="list-style-type: none"> ● Doppler functional capability SD-120 accomplished concurrently with SD-118 & SD-119	<ul style="list-style-type: none"> ● High-Frequency Mode <ul style="list-style-type: none"> ● High data rate with & without ranging ● Low data rate

⁽¹⁾ All parameters to be tested as a function of RF total received power.

Table 4.23. Orbiter-STDN Direct PM S-Band STDN Test Procedure

STDN PM Direct Link ESTL Test Procedure Section	TRAS No.	Link	Channel to be Tested	Type of Test
5.2.1.1.1	SD-101	PM uplink (Forward link)	TDM	Uplink BER and AGC voltage verification--daily measurement
5.2.1.2.1	SD-101 & SD-102	PM uplink (Forward link)	TDM	Bit error rate (active voice and commands)
5.2.1.2.2	SD-101 & SD-102	PM uplink (Forward link)	TDM	Bit error rate (inactive voice and commands)
5.2.1.2.3	SD-102 & SD-103	PM uplink (Forward link)	TDM	Percent data loss
5.2.1.3.1	SD-104 & SD-105	PM uplink (Forward link)	Command	Message rejection rate (active voice)
5.2.1.3.2	SD-104 & SD-105	PM uplink (Forward link)	Command	Message rejection rate (inactive voice)
5.2.1.3.3	SD-104 & SD-105	PM uplink (Forward link)	Command	Verification of receipt of 10,000 error-free commands
5.2.1.4.1	SD-106 & SD-111	PM uplink (Forward link)	Voice	Bit error rate
5.2.1.4.2	SD-106 & SD-111	PM uplink (Forward link)	Voice	Postdetection SNR (ATU output)

Table 4.23. Orbiter-STDN Direct PM S-Band STDN Test Procedure
(Cont'd)

STDN PM Direct Link ESTL Test Procedure Section	TRAS No.	Link	Channel to be Tested	Type of Test
5.2.1.4.3	SD-106 & SD-111	PM uplink (Forward link)	Voice	Postdetection SNR (AIU output)
5.2.1.4.4	SD-106 & SD-111	PM uplink (Forward link)	Voice	Postdetection SP/N ratio (ATU output)
5.2.1.4.5	SD-106 & SD-111	PM uplink (Forward link)	Voice	Postdetection SP/N ratio (AIU output)
5.2.1.4.6	SD-106 & SD-111	PM uplink (Forward link)	Voice	Postdetection SP/N ratio (ATU output)--MCC/ GSTDN site/return loop voice
5.2.1.4.7	SD-106 & SD-111	PM uplink (Forward link)	Voice	Subjective voice quality (ATU output)--active commands
5.2.1.4.8	SD-106 & SD-111	PM uplink (Forward link)	Voice	Subjective voice quality (ATU output)
5.2.1.4.9	SD-106 & SD-111	PM uplink (Forward link)	Voice	Subjective voice quality (AIU output)
5.2.1.4.10	SD-106 & SD-111	PM uplink (Forward link)	Voice	Subjective voice quality (SMU output)
5.2.1.4.11	SD-106 & SD-111	PM uplink (Forward link)	Voice	Subjective voice quality (ATU output)--MCC/ GSTDN site/return loop voice
5.2.1.4.12	SD-106 & SD-111	PM uplink (Forward link)	Voice	Word intelligibility (ATU output)

**Table 4.23. Orbiter-STDN Direct PM S-Band STDN Test Procedure
(Cont'd)**

STDN PM Direct Link ESTL Test Procedure Section	TRAS No.	Link	Channel to be Tested	Type of Test
5.2.1.4.13	SD-106 & SD-111	PM uplink (Forward link)	Voice	Word intelligibility (AIU output)
5.2.1.4.14	SD-106 & SD-111	PM uplink (Forward link)	Voice	Word intelligibility (ATU output)--MCC/GSTDN site/return loop voice
5.2.2.2.1	SD-107	PM downlink (Return link)	TDM	Bit error rate (active voice)
5.2.2.2.2	SD-107	PM downlink (Return link)	TDM	Bit error rate (inactive voice)
5.2.2.2.3	SD-107	PM downlink (Return link)	TDM	Bit error rate (inactive voice)--effects of
5.2.2.2.4.1	SD-108 & SD-110	PM downlink (Return link)	TDM	Evaluation of frame sync strategy--330 bit sync/403 frame sync combination
5.2.2.2.4.2	SD-108 & SD-110	PM downlink (Return link)	TDM	Percent data loss (active voice)--330 bit sync/403 frame sync combination
5.2.2.2.5.1	SD-108 & SD-110	PM downlink (Return link)	TDM	Evaluation of frame sync strategy--317D bit sync/MSFTP-II decom system combination
5.2.2.2.5.2	SD-108 & SD-110	PM downlink (Return link)	TDM	Percent data loss (active voice)--317D bit sync/MSFTP-II decom system combination
5.2.2.3.1	SD-108 & SD-109	PM downlink (Return link)	Telemetry	Bit error rate (inactive voice)

Table 4.23. Orbiter-STDN Direct PM S-Band STDN Test Procedure
(Cont'd)

STDN PM Direct Link ESTL Test Procedure Section	TRAS No.	Link	Channel to be Tested	Type of Test
5.2.2.4.1	SD-110 & SD-111	PM Downlink (Return link)	Voice	Bit error rate
5.2.2.4.2	SD-110 & SD-111	PM Downlink (Return link)	Voice	Postdetection SNR (ATU input)
5.2.2.4.3	SD-110 & SD-111	PM downlink (Return link)	Voice	Postdetection SNR (AIU input)
5.2.2.4.4	SD-110 & SD-111	PM downlink (Return link)	Voice	Postdetection SP/N ratio (ATU input)
5.2.2.4.5	SD-110 & SD-111	PM downlink (Return link)	Voice	Postdetection SP/N ratio (ATU input)--MCC/ GSTDN site/return loop voice
5.2.2.4.6	SD-110 & SD-111	PM downlink (Return link)	Voice	Postdetection SP/N ratio (ATU input)--MCC/ GSTDN site/return loop voice
5.2.2.4.7	SD-110 & SD-111	PM downlink (Return link)	Voice	Subjective voice quality (ATU input)
5.2.2.4.8	SD-110 & SD-111	PM downlink (Return link)	Voice	Subjective voice quality (AIU input)
5.2.2.4.9	SD-110 & SD-111	PM downlink (Return link)	Voice	Subjective voice quality (SMU input)
5.2.2.4.10	SD-110 & SD-111	PM downlink (Return link)	Voice	Subjective voice quality (ATU input)--MCC/ GSTDN site/return loop voice

Table 4.23. Orbiter-STDN Direct PM S-Band STDN Test Procedure
(Cont'd)

STDN PM Direct Link ESTL Test Procedure Section	TRAS No.	Link	Channel to be Tested	Type of Test
5.2.2.4.11	SD-110 & SD-111	PM downlink (Return link)	Voice	Word intelligibility (ATU input)
5.2.2.4.12	SD-110 & SD-111	PM downlink (Return link)	Voice	Word intelligibility (AIU input)
5.2.2.4.13	SD-110 & SD-111	PM downlink (Return link)	Voice	Word intelligibility (ATU input)--MCC/GSTDN site/return loop voice
5.2.3.1.1	SD-112	PM uplink (Forward link)	RF Carrier	RF acquisition time
5.2.3.2.1	SD-113	PM downlink (Return link)	RF Carrier	RF acquisition time
5.2.3.3.1	SD-112 & SD-113	Two-way	RF Carrier	RF acquisition
5.2.3.3.2	SD-113, -114 & -115	Two-way	RF Carrier	RF acquisition/mode switching
5.2.3.3.3	SD-112 & SD-113	Two-way	RF	Carrier tracking threshold
5.2.3.3.4	SD-113 -114 & -115	Two-way	RF Carrier	RF acquisition (dynamic doppler)
5.2.4.1	SD-116	Two-way	Ranging	Ranging subcarrier predetection SNR

**Table 4.23. Orbiter-STDN Direct PM S-Band STDN Test Procedure
(Cont'd)**

STDN PM Direct Link ESTL Test Procedure Section	TRAS No.	Link	Channel to be Tested	Type of Test
5.2.4.2	SD-116	Two-way	Ranging	Ranging tone postdetection S/N
5.2.4.3	SD-116 & SD-117	Two-way	Ranging	3 σ ranging error and range acquisition time
5.2.5.1.1	SD-102 -103 & -118	Uplink (Forward link)	One-way Doppler	Doppler accuracy
5.2.5.2.1	SD-119 & SD-120	Two-way	Two-way Doppler	Doppler accuracy

Table 4.24. STDN Test Procedure versus Operational Modes

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STDN PM Direct Link ESTL Test Procedure Section	Test	STDN Mode										STDN High-Power Mode									
		Low Frequency					High Frequency					Low Frequency					High Frequency				
		Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)
		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng	
5.2.1.1.1	Uplink BER and AGC Voltage Verification Daily Measurement <ul style="list-style-type: none"> NSP - DOD Mode, No Voice NSP - NASA Mode, No Voice 								X												
5.2.1.2.1	Uplink TDM Channel - Bit Error Rate (Active Voice and Commands) <ul style="list-style-type: none"> NSP - DOD Mode NSP - NASA Mode 								X												
5.2.1.2.2	Uplink TDM Channel - Bit Error Rate (Inactive Voice and Commands) <ul style="list-style-type: none"> NSP - DOD Mode, Receive Only Mode, Power Amplifier Off -Both FM Xmtrs Off, 0 Doppler ±60 kHz Doppler -OI FM Xmtr On, (-40 dB Coupling Loss (Tested at 0 Doppler) (-50 dB Coupling Loss (-60 dB Coupling Loss -DFI FM Xmtr On, (-40 dB Coupling Loss (Tested at 0 Doppler) (-50 dB Coupling Loss (-60 dB Coupling Loss -Both FM Xmtrs On, (-40 dB Coupling Loss (Tested at 0 Doppler) (-50 dB Coupling Loss (-60 dB Coupling Loss NSP - DOD Mode, Receive Only Mode, Power Amplifier On No Tests Conducted NSP - DOD Mode, Xpond Mode, Power Amplifier Off -Both FM Xmtrs Off, 0 Doppler ±60 kHz Doppler -OI FM Xmtr On, (-40 dB Coupling Loss (Tested at 0 Doppler) (-50 dB Coupling Loss (-60 dB Coupling Loss -DFI FM Xmtr On, (-40 dB Coupling Loss (Tested at 0 Doppler) (-50 dB Coupling Loss (-60 dB Coupling Loss -Both FM Xmtrs On, (-40 dB Coupling Loss (Tested at 0 Doppler) (-50 dB Coupling Loss (-60 dB Coupling Loss 	X	X	X	X		X	X	X	X				X						X	
		X	X	X	X		X	X	X	X				X						X	
		X	X	X	X		X	X	X	X				X					X	X	
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														X							

NSP-DOD mode \equiv Encrypted
NSP-NASA mode \equiv Clear

Table 4.24. STDN Test Procedure versus Operational Modes (Cont'd)

STDR FM Direct Link ESTL Test Procedure Section	Test	STDN Mode										STDN High-Power Mode									
		Low Frequency					High Frequency					Low Frequency					High Frequency				
		Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)
		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng	
5.2.1.4.3	Uplink Voice Channel - Postdetection SNR (Audio Interface Unit Output) <ul style="list-style-type: none"> NSP - DOD Mode (No Tests Conducted) NSP - NASA Mode/ACCU Output Enabled -Voice 1 (AIU-L) -Voice 2 (AIU-R) 																				
5.2.1.4.4	Uplink Voice Channel - Postdetection SP/N Ratio (Audio Terminal Unit Output) <ul style="list-style-type: none"> NSP - DOD Mode (No Tests Conducted) NSP - NASA Mode/ACCU Output Enabled -ATU-L (Voice 1) -ATU-R (Voice 2) 								X												
5.2.1.4.5	Uplink Voice Channel - Postdetection SP/N Ratio (Audio Interface Unit Output) <ul style="list-style-type: none"> NSP - DOD Mode (No Tests Conducted) NSP - NASA Mode/ACCU Output Enabled -Voice 1 (AIU-L) -Voice 2 (AIU-R) 						X	X	X	X											
5.2.1.4.6	Uplink Voice Channel - Postdetection SP/N Ratio (Audio Terminal Unit Output) -MCC/GSTDN Site/Return Loop Voice <ul style="list-style-type: none"> NSP - DOD Mode (No Tests Conducted) NSP - NASA Mode/ACCU Output Enabled -ATU-L (Voice 1) -ATU-R (Voice 2) 								X												
	Uplink Voice Channel - Subjective Voice Quality (Audio Terminal Unit Output) <ul style="list-style-type: none"> NSP - DOD Mode (No Tests Conducted) NSP - NASA Mode/ACCU Output Enabled 								X	X											
5.2.1.4.7	-ATU-L (Voice 1) Active Commands -ATU-R (Voice 2) Active Commands								X												
5.2.1.4.8	-ATU-L (Voice 1) Inactive Commands -ATU-R (Voice 2) Inactive Commands						X	X	X	X											

Table 4.24. STDN Test Procedure versus Operational Modes (Cont'd)

STN FM Direct Link ESTL Test Procedure Section	Test	STDN Mode										STDN High-Power Mode									
		Low Frequency					High Frequency					Low Frequency					High Frequency				
		Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)
		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng	
5.2.1.4.3	Uplink Voice Channel - Postdetection SNR (Audio Interface Unit Output) • NSP - DND Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Output Enabled -Voice 1 (ATU-L) -Voice 2 (ATU-R)																				
5.2.1.4.4	Uplink Voice Channel - Postdetection SP/N Ratio (Audio Terminal Unit Output) • NSP - DND Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Output Enabled -ATU-L (Voice 1) -ATU-R (Voice 2)									X											
5.2.1.4.5	Uplink Voice Channel - Postdetection SP/N Ratio (Audio Interface Unit Output) • NSP - DND Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Output Enabled -Voice 1 (ATU-L) -Voice 2 (ATU-R)																				
5.2.1.4.6	Uplink Voice Channel - Postdetection SP/N Ratio (Audio Terminal Unit Output) -MCC/GSTDN Site/Return Loop Voice • NSP - DND Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Output Enabled -ATU-L (Voice 1) -ATU-R (Voice 2) Uplink Voice Channel - Subjective Voice Quality (Audio Terminal Unit Output) • NSP - DND Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Output Enabled -ATU-L (Voice 1) Active Commands -ATU-R (Voice 2) Active Commands																				
5.2.1.4.7	-ATU-L (Voice 1) Inactive Commands -ATU-R (Voice 2) Inactive Commands																				
5.2.1.4.8																					

Table 4.24. STDN Test Procedure versus Operational Modes (Cont'd)

4

STDN PM Direct Link ESTL Test Procedure Section	Test	STDN Mode										STDN High-Power Mode											
		Low Frequency					High Frequency					Low Frequency					High Frequency						
		Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)		
		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng
5.2.1.4.9	Uplink Voice Channel - Subjective Voice Quality (Audio Interface Unit Output) <ul style="list-style-type: none">• NSP - DOD Mode (No Tests Conducted)• NSP - NASA Mode/ACCU Output Enabled-Voice 1 (AIU-L)-Voice 2 (AIU-R)																						
5.2.1.4.10	Uplink Voice Channel - Subjective Voice Quality (Speaker Microphone Unit Output) <ul style="list-style-type: none">• NSP - DOD Mode (No Tests Conducted)• NSP - NASA Mode/ACCU Output Enabled-Voice 1 (SMU-L)-Voice 2 (SMU-R)																						
5.2.1.4.11	Uplink Voice Channel - Subjective Voice Quality (Audio Terminal Unit Output) - MCC/GSTDN Site/Return Loop Voice <ul style="list-style-type: none">• NSP - DOD Mode (No Tests Conducted)• NSP - NASA Mode/ACCU Output Enabled-ATU-L (Voice 1)-ATU-R (Voice 2)																						
5.2.1.4.12	Uplink Voice Channel - Word Intelligibility (Audio Terminal Unit Output) <ul style="list-style-type: none">• NSP - DOD Mode (No Tests Conducted)• NSP - NASA Mode/ACCU Output Enabled-ATU-L (Voice 1)-ATU-R (Voice 2)																						
5.2.1.4.13	Uplink Voice Channel - Word Intelligibility (Audio Interface Unit Output) <ul style="list-style-type: none">• NSP - DOD Mode (No Tests Conducted)• NSP - NASA Mode/ACCU Output Enabled-Voice 1 (AIU-L)-Voice 2 (AIU-R)																						
5.2.1.4.14	Uplink Voice Channel - Word Intelligibility (Audio Terminal Unit Output) - MCC/GSTDN Site/Return Loop Voice <ul style="list-style-type: none">• NSP - DOD Mode (No Tests Conducted)• NSP - NASA Mode/ACCU Output Enabled-ATU-L (Voice 1)-ATU-R (Voice 2)																						

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Table 4.24. STDN Test Procedure versus Operational Modes (Cont'd)

5

STDN PM Direct Link ESTL Test Procedure Section	Test	STDN Mode										STDN High-Power Mode									
		Low Frequency					High Frequency					Low Frequency					High Frequency				
		Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)
		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng	
5.2.2.2.1	Downlink TDM Channel ^a - Bit Error Rate (Active Voice) <ul style="list-style-type: none"> NSP - DOD Mode/ACCU Output Enabled -BER/330 Bit Sync Output -BER/317D Bit Sync Output 								X												
5.2.2.2.2	Downlink TDM Channel ^a - Bit Error Rate (Inactive Voice) <ul style="list-style-type: none"> NSP - DOD Mode/ACCU Output Enabled -330 Bit Sync Output <ul style="list-style-type: none"> Both FM Xmtrs Off, 0 Doppler 01 FM Xmtr On, 0 Doppler DFI FM Xmtr On, 0 Doppler Both FM Xmtrs On, 0 Doppler -317D Bit Sync Output <ul style="list-style-type: none"> Both FM Xmtrs Off, 0 Doppler FM Xmtrs On (No Tests Conducted) NSP - NASA Mode (No Tests Conducted) 	X	X	X ^b	X ^b		X	X	X ^b	X ^b				X	X				X	X	
5.2.2.2.3	Downlink TDM Channel ^a - Bit Error Rate (Inactive Voice) - Effects of MFR Channel Gain Differences <ul style="list-style-type: none"> NSP - DOD Mode/ACCU Output Enabled -330 Bit Sync Output <ul style="list-style-type: none"> CHA = CHB Power^c CHA 6 dB > CHB^c CHA 10 dB > CHB^c CHA 16 dB > CHB^c CHA 20 dB > CHB^c All Power in CHA^c -317D Bit Sync Output (No Tests Conducted) NSP - NASA Mode (No Tests Conducted) 								X												

^aFor all downlink tests, the uplink modulated with corresponding signal combination, unless noted.^bConducted with and without uplink modulation.^cAt various attenuator settings.

Table 4.24. STDN Test Procedure versus Operational Modes (Cont'd)

6

STDN PM Direct Link ESTL Test Procedure Section	Test	STDN Mode										STDN High-Power Mode									
		Low Frequency					High Frequency					Low Frequency					High Frequency				
		Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)
		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng	
5.2.2.2.4.1	Downlink TDM Channel ^a - Evaluation of Frame Sync Strategy - 330 Bit Sync/403 Frame Sync Combination																				
	• NSP - ?																				
	-Four Frame Sync Strategy Settings								X												
5.2.2.2.4.2	Downlink TDM Channel ^a - Percent Data Loss (Active Voice) - 330 Bit Sync/403 Frame Sync Combination																				
	• NSP - ?						X	X	X	X											
5.2.2.2.5.1	Downlink TDM Channel ^a - Evaluation of Frame Sync Strategy - 317D Bit Sync/MSFTP-II DECOM System Combination																				
	• NSP - ?																				
	-Four Frame Sync Strategy Settings								X												
5.2.2.2.5.2	Downlink TDM Channel ^a - Percent Data Loss (Active Voice) - 317D Bit Sync/MSFTP-II																				
	• NSP - ?						X	X	X	X											
5.2.2.3.1	Downlink Telemetry Channel ^a - Bit Error Rate																				
	• NSP - ? Active Voice						X	X	X	X											
	Inactive Voice																				
5.2.2.4.1	Downlink Voice Channel ^a - Bit Error Rate																				
	• NSP - DOD Mode/PSS Enable On																				
	-Voice 1 (DEMUX)						X	X	X	X											
	-Voice 2 (DEMUX)								X	X											
	• NSP - NASA Mode (No Tests Conducted)																				
5.2.2.4.2	Downlink Voice Channel ^a - Postdetection SNR (Audio Terminal Unit Input)																				
	• NSP - DOD Mode (No Tests Conducted)																				
	• NSP - NASA Mode/ACCU Enable On																				
	-Voice 1 (Down)						X	X	X	X											
	-Voice 2 (Down)								X	X											

^aFor all downlink tests, the uplink modulated with corresponding signal combination, unless noted.

Table 4.24. STDN Test Procedure versus Operational Modes (Cont'd)

7

STDN PM Direct Link ESTL Test Procedure Section	Test	STDN Mode										STDN High-Power Mode									
		Low Frequency					High Frequency					Low Frequency					High Frequency				
		Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)
		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng	
5.2.2.4.3	Downlink Voice Channel ^a - Postdetection SNR (Audio Interface Unit Input) • NSP - DOD Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Enable On -Voice 1 (Down) -Voice 2 (Down)																				
									X												
5.2.2.4.4	Downlink Voice Channel ^a - Postdetection SP/N Ratio (Audio Terminal Unit Input) • NSP - DOD Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Enable On -Voice 1 (Down) -Voice 2 (Down)																				
							X	X	X	X											
5.2.2.4.5	Downlink Voice Channel ^a - Postdetection SP/N Ratio (Audio Interface Unit Input) • NSP - DOD Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Enable On -Voice 1 (Down) -Voice 2 (Down)																				
									X												
5.2.2.4.6	Downlink Voice Channel ^a - Postdetection SP/N Ratio (Audio Terminal Unit Input) - MCC/GSTDN Site/Return Loop Voice • NSP - DOD Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Enable On -Voice 1 (Down) -Voice 2 (Down)																				
							X	X	X	X											
5.2.2.4.7	Downlink Voice Channel ^a - Subjective Voice Quality (Audio Terminal Unit Input) • NSP - DOD Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Enable On -Voice 1 (Down) -Voice 2 (Down)																				
							X	X	X	X											

^aFor all downlink tests, the uplink modulated with corresponding signal combination, unless noted.

Table 4.24. STDN Test Procedure versus Operational Modes (Cont'd)

8

STDN PM Direct Link ESTL Test Procedure Section	Test	STDN Mode										STDN High-Power Mode									
		Low Frequency					High Frequency					Low Frequency					High Frequency				
		Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)	Lo Data		Hi Data		No Data (C.O.)
		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng		W/O Rng	W/ Rng	W/O Rng	W/ Rng	
5.2.2.4.8	Downlink Voice Channel ^a - Subjective Voice Quality (Audio Interface Unit Input) • NSP - DOD Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Enable On -Voice 1 (Down) -Voice 2 (Down)																				
5.2.2.4.9	Downlink Voice Channel ^a - Subjective Voice Quality (Speaker Microphone Unit Input) • NSP - DOD Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Enable On -Voice 1 (Down) -Voice 2 (Down)								X												
5.2.2.4.10	Downlink Voice Channel ^a - Subjective Voice Quality (Audio Terminal Unit Input) - MCC/GSTDN Site/Return Loop Voice • NSP - DOD Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Enable On -Voice 1 (Down) -Voice 2 (Down)																				
5.2.2.4.11	Downlink Voice Channel ^a - Word Intelligibility (Audio Terminal Unit Input) • NSP - DOD Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Enable On -Voice 1 (Down) -Voice 2 (Down)						X	X	X	X											
5.2.2.4.12	Downlink Voice Channel ^a - Word Intelligibility (Audio Interface Unit Input) • NSP - DOD Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Enable On -Voice 1 (Down) -Voice 2 (Down)						X	X	X	X											

^aFor all downlink tests, the uplink modulated with corresponding signal combination, unless noted.REPRODUCIBILITY OF THE
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Table 4.24. STDN Test Procedure versus Operational Modes (Cont'd)

STDN PM Direct Link ESTL Test Procedure Section	Test	STDN Mode												STDN High-Power Mode													
		Low Frequency						High Frequency						Low Frequency						High Frequency							
		Lo Data			Hi Data			Lo Data			Hi Data			Lo Data			Hi Data			Lo Data			Hi Data				
		W/O Rng	W/ Rng	No Data (C.O.)	W/O Rng	W/ Rng	No Data (C.O.)	W/O Rng	W/ Rng	No Data (C.O.)	W/O Rng	W/ Rng	No Data (C.O.)	W/O Rng	W/ Rng	No Data (C.O.)	W/O Rng	W/ Rng	No Data (C.O.)	W/O Rng	W/ Rng	No Data (C.O.)					
5.2.2.4.13	Downlink Voice Channel ^a - Word Intelligibility (Audio Interface Unit Input) - MCC/GSTDN Site/ Return Loop Voice • NSP - DOD Mode (No Tests Conducted) • NSP - NASA Mode/ACCU Enable On -Voice 1 (Down) -Voice 2 (Down)																										
5.2.3.1.1	Uplink RF Acquisition Time • 0 kHz Doppler Shift • ±20 kHz Doppler Shift • ±40 kHz Doppler Shift • ±60 kHz Doppler Shift																										
5.2.3.2.1	Downlink RF Acquisition Time ^a																										
5.2.3.3.1	Two-Way RF Acquisition Test • 0 kHz Doppler Shift (Uplink) • ±20 kHz Doppler Shift (Uplink) • ±40 kHz Doppler Shift (Uplink) • ±60 kHz Doppler Shift (Uplink)																										
5.2.3.3.2	Two-Way RF Acquisition/Mode Switching ^d • 0 kHz Doppler Shift (Uplink) • ±60 kHz Doppler Shift (Uplink)																										
5.2.3.3.3	Two-Way Carrier Tracking Threshold • 0 kHz Doppler Shift (Uplink) • ±60 kHz Doppler Shift (Uplink)																										
5.2.3.3.4	Two-Way RF Acquisition (Dynamic Doppler) • ±10 kHz Doppler Offset - 2 kHz/sec Rate • ±20 kHz Doppler Offset - 4 kHz/sec Rate																										

^aFor all downlink tests, the uplink modulated with corresponding signal combination, unless noted.
^bUplink remains carrier only.
^cUplink (UL) and downlink (DL) signal combinations different
^dSwitching from one mode to another.

10

[illegible]

Generally, the STDN S-band PM direct link test procedures meet the TRAS requirements. The procedures appear to be well thought out, well-written and very complete. It should be noted that the STDN TRAS report was written in September 1977 and the STDN PM direct link test procedures were written in June 1978. Many of the STDN direct link tests have been recently completed in the ESTL; however, there has been a significant time period between completing the documentation and conducting the tests. During this time period, a number of equipment operating parameters have been changed which are not reflected in the STDN TRAS reports or the STDN procedures. The ESTL personnel are aware of many of these changes, have in some instances modified the tests to reflect the current situation but have no plans to formally change the documentation. Therefore, many of the comments discussed in this report have already been addressed by the appropriate ESTL personnel.

The STDN PM direct link test procedure comments are divided into two sections. The first section concerns the test parameters and equipment used and the second section compares specific tests with the corresponding TRAS number.

4.4.3.1 General STDN test procedure comments

In reviewing the STDN S-band ESTL test procedure, there are four comments concerning the test parameters and equipment used. The four comments are:

(1) On pages III-4 and III-5 describing the uplink and down-link signal performance requirements, respectively, the PM modulation indices have been changed because of interference on the ranging channel. Also, the required Prec/No has been changed as documented in "Space Shuttle Communications and Tracking Link Circuit Margin Summary," April 1979, EH2-M79-039, and will be reflected in ICD 2-OD004 in the next revision (PRIN 14). On page III-4, 66.0 dB-Hz s/b 61.8 dB-Hz for combination 25 and s/b 58.3 dB-Hz for combination 25A. On page III-5, 63.7 dB-Hz s/b 68.3 dB-Hz, 60.7 dB-Hz s/b 65.3 dB-H, 66.0 dB-Hz s/b 70.7 dB-Hz for combination 3 and s/b 67.7 dB for combination 4.

(2) On page III-6 and throughout the remainder of the test procedure, the maximum doppler offset specified is ± 60 kHz; however, in the latest network transponder specification, RI Specification MC 478-0106 Rev. E, Seq. 04, the ± 60 kHz has been changed to ± 55 kHz.

(3) It should be noted that the doppler extractor (DE) has been eliminated from the S-band system; however, the DE is required for the ESTL to perform a number of tests. The point is that the DE which the ESTL possesses is no longer being evaluated as part of the S-band system but is being used as a piece of test equipment.

(4) In some tests, the NSP is in the DOD mode while, in other tests, the NSP is in the NASA mode. When the STDN procedures were written, the DOD mode indicated encrypted operations and the NASA mode indicated clear or nonencrypted operations. Since the STDN operational mode is strictly NASA, it would seem illogical that a portion of the tests were to be conducted in the DOD mode.

The apparent illogic is really a moot point because, since the STDN procedures were written, a number of operational changes have evolved. For uplink operations, both the DOD and NASA modes will now be encrypted and, for downlink operations, the DOD mode will now be encrypted while the NASA mode now may or may not be encrypted. For the purposes of this report, however, DOD mode will still mean encrypted and NASA mode will still mean clear or nonencrypted.

The comment is that some of the ESTL tests no longer reflect current operational practices. For example, there are a number of STDN uplink tests that are in the clear mode when the encrypted mode should be used. It would be desirable to reconduct some tests.

4.4.3.2 Specific STND tests/TRAS comments

Table 4.25 summarizes the comments resulting from comparing the specific ESTL STDN tests with the TRAS requirements. Some of the comments have already been discussed in the previous section, such as the change in the required Prec/No, the new doppler maximum offsets and the NSP being tested in either the DOD or NASA mode. There are, however, some new comments such as mean-time-to-unlock and carrier-to-noise ratio tests not being conducted as required by the TRAS and the acquisition time changing as a result of a network transponder performance specification change.

Table 4.25. Tests versus TRAS

STDN PM Direct Link ESTL Test Procedure Section	TRAS No.	Test Procedure Comments
5.2.1.1.1	SD-101	● NSP tested in DOD mode only
5.2.1.2.1	SD-101 and SD-102	● NSP tested in DOD mode only
5.2.1.2.2	SD-101 and SD-102	<ul style="list-style-type: none"> ● NSP tested in DOD mode only ● ± 60 kHz doppler offset outside of transponder specification of ± 55 kHz ● Prec/No = 66.0 dB-Hz used for the high and low data rates, with ranging, success criteria has been changed to 61.8 dB-Hz and 58.3 dB-Hz, respectively.
5.2.1.2.3	SD-102 and SD-103	● OK
5.2.1.3.1 and 5.2.1.3.2	SD-104 and SD-105	● BER's cannot be measured for the command channel (test points not available). Decoded command channel serial BER extrapolated using message rejection rate data.
5.2.1.3.3	SD-104 and SD-105	● OK
5.2.1.4.1	SD-106 and SD-111	● NSP tested in DOD mode only
5.2.1.4.2 5.2.1.4.3 5.2.1.4.4 5.2.1.4.5 5.2.1.4.6 5.2.1.4.7 5.2.1.4.8 5.2.1.4.9 5.2.1.4.10 5.2.1.4.11 5.2.1.4.12 5.2.1.4.13 5.2.1.4.14	SD-106 and SD-111	● NSP tested in NASA mode only

NSP-DOD mode \equiv Encrypted
 NSP-NASA mode \equiv Clear

Table 4.25. Tests versus TRAS (Cont'd)

STDN PM Direct Link ESTL Test Procedure Section	TRAS No.	Test Procedure Comments
-	SD-106 and SD-111	Percent data loss not performed specifically for uplink voice channel
5.2.2.2.1	SD-107	<ul style="list-style-type: none"> ● NSP tested in DOD mode only ● PREC/No = 63.7 dB-Hz; s/b 68.3 dB-Hz
5.2.2.2.2	SD-107	<ul style="list-style-type: none"> ● NSP tested in DOD mode only ● ± 60 kHz doppler offset outside of transponder specification of ± 55 kHz ● PREC/No = 63.7 dB-Hz; s/b 68.3 dB-Hz ● PREC/No = 60.7 dB-Hz; s/b 65.3 dB-Hz ● PREC/No = 66.0 dB-Hz; s/b 70.7 dB-Hz for combination 3 and 67.7 dB-Hz for combination 4
5.2.2.2.3	SD-107	<ul style="list-style-type: none"> ● NSP tested in DOD mode only
5.2.2.2.4.1 5.2.2.2.4.2 5.2.2.2.5.1 5.2.2.2.5.2	SD-108 and SD-110	<ul style="list-style-type: none"> ● NSP mode not specified
5.2.2.3.1	SD-108 and SD-109	<ul style="list-style-type: none"> ● NSP mode not specified ● PREC No = 63.7 dB-Hz; s/b 68.3 dB-Hz ● PREC/No = 60.7 dB-Hz; s/b 65.3 dB-Hz ● PREC/No = 66.0 dB-Hz; s/b 70.7 dB-Hz for combination 3 and 67.7 dB-Hz for combination 4
5.2.2.4.1	SD-110 and SD-111	<ul style="list-style-type: none"> ● NSP tested in DOD mode only

NSP-DOD mode \equiv Encrypted
 NSP-NASA mode \equiv Clear

Table 4.25. Tests versus TRAS (Cont'd)

STDN PM Direct Link ESTL Test Procedure Section	TRAS No.	Test Procedure Comments
5.2.2.4.2 5.2.2.4.3 5.2.2.4.4 5.2.2.4.5 5.2.2.4.6 5.2.2.4.7 5.2.2.4.8 5.2.2.4.9 5.2.2.4.10	SD-110 and SD-111	<ul style="list-style-type: none"> ● NSP tested in NASA mode only
5.2.2.4.11	SD-110 and SD-111	<ul style="list-style-type: none"> ● NSP tested in NASA mode only ● PREC/No = 63.7 dB-Hz; s/b 68.3 dB-Hz ● PREC/No = 60.7 dB-Hz; s/b 65.3 dB-Hz ● PREC/No = 66.0 dB-Hz; s/b 70.7 dB-Hz for combination 3 and 67.7 dB-Hz for combination 4
5.2.2.4.12	SD-110 and SD-111	<ul style="list-style-type: none"> ● NSP tested in NASA mode only ● PREC/No = 63.7 dB-Hz; s/b 68.3 dB-Hz
5.2.2.4.13	SD-110 and SD-111	<ul style="list-style-type: none"> ● NSP tested in NASA mode only ● PREC/No = 63.7 dB-Hz; s/b 68.3 dB-Hz ● PREC/No = 60.7 dB-Hz; s/b 65.3 dB-Hz ● PREC/No = 66.0 dB-Hz; s/b 70.7 dB-Hz for combination 3 and 67.7 dB-Hz for combination 4
-	SD-110 and SD-111	Percent data loss not performed specifically for downlink voice channel
5.2.3.1.1	SD-112	<ul style="list-style-type: none"> ● ± 60 kHz doppler offset; s/b ± 55 kHz ● 4-second acquisition time; s/b 6 seconds ● Mean-time-to-uplink and carrier-to-noise ratio tests not conducted ● High-frequency mode, high data rate with ranging tests not conducted.

NSP-DOD mode \equiv EncryptedNSP-NASA mode \equiv Clear

Table 4.25. Tests versus TRAS (Cont'd)

STDN PM Direct Test ESTL Test Procedure Section	TRAS No.	Test Procedure Comments
5.2.3.2.1	SD-113	<ul style="list-style-type: none"> ● ± 60 kHz doppler offset; s/b ± 55 kHz ● The downlink tests with the ranging channel enabled cannot be performed as described with only the carrier present on the uplink ● Mean-time-to-unlock and carrier-to-noise ratio tests not conducted
5.2.3.3.1	SD-113 SD-114 and SD-115	<ul style="list-style-type: none"> ● ± 60 kHz doppler offset; s/b ± 55 kHz ● The 8-second two-way acquisition time s/b 10 seconds (6-second uplink acquisition + 4-second downlink acquisition)
5.2.3.3.2 5.2.3.3.3	SD-112 and SD-113	<ul style="list-style-type: none"> ● ± 60 kHz doppler offset; s/b ± 55 kHz
5.2.3.3.4	SD-113 SD-114 and SD-115	<ul style="list-style-type: none"> ● Maximum transponder specification doppler rate is ± 5 kHz/s; maximum test rate is -4 kHz/s.
5.2.4.1	SD-116	<ul style="list-style-type: none"> ● 1.0 radian modulation index as specified has been changed
5.2.4.2	SD-116	<ul style="list-style-type: none"> ● 0.6 radian modulation index as specified has been changed
5.2.4.3	SD-116 and SD-117	<ul style="list-style-type: none"> ● $\text{PREC}/N_o \geq 66.0$ dB-Hz; s/b 61.8 dB-Hz for uplink and 70.7 dB-Hz for downlink ● ± 60 kHz doppler offset; s/b ± 55 kHz
5.2.5.1.1	SD-102 SD-103 and SD-118	<ul style="list-style-type: none"> ● $\text{PREC}/N_o = 66.0$ dB-Hz; s/b 61.8 dB-Hz ● ± 60 kHz doppler offset; s/b ± 55 kHz
5.2.5.2.1	SD-119 and SD-120	<ul style="list-style-type: none"> ● PREC/N_o (up) ≥ 66.0 dB-Hz; s/b 61.8 dB-Hz ● PREC/N_o (down) ≥ 63.7 dB-Hz; s/b 68.3 dB-Hz ● PREC/N_o (down) ≥ 60.7 dB-Hz; s/b 65.3 dB-Hz ● PREC/N_o (down) ≥ 66.0 dB-Hz; s/b 70.7 dB-Hz ● ± 60 kHz doppler offset; s/b ± 55 kHz

NSP-DOD mode \equiv Encrypted
 NSP-NASA mode \equiv Clear

4.4.4 Conclusions

Overall, the STDN test procedures are well thought out, well-written and generally meet the TRAS requirements. Of the comments outlined in this report, most have been addressed by the ESTL personnel even though the ESTL has no plans to formally change the test procedure documentation.

The major concern, of course, is the STDN tests that have been conducted with the NSP in a mode that no longer reflects the current operational practices. It is recommended that at least some tests be reconducted with the NSP in the proper mode in order to assure that the equipment will meet mission requirements.

As previously stated, Axiomatix possesses all three TRAS reports: STDN, TDRS and AF/SCF (SGLS). Axiomatix has requested all three corresponding test procedures but NASA has supplied only the STDN procedures. This report, therefore, has evaluated only the STDN procedures and Axiomatix will require the other two procedures should NASA desire a similar evaluation.

4.5 Peak Regulator Design and Performance

During the first quarter of 1979 and prior to the decision being made to use the PI internal RMS type regulator for the wideband bent-pipe signal amplitude control (see subsection 3.2.6), Axiomatix pursued a laboratory investigation of the performance of a signal-peak type regulator. The purpose for this activity was twofold:

- (1) To demonstrate the simplicity of implementation using readily available integrated circuits
- (2) To show that the peak regulating loop would be stable and perform to expectations for all input waveforms.

Figure 4.16 is a circuit diagram for the Axiomatix peak regulator breadboard, and Figure 4.17 shows the companion timing logic circuits. Most of the regulator design is based upon operational amplifier configurations. The amplifiers having the AD prefix are Analog Device types, and AD583 is the sample/hold amplifier. Block AH0152 is a FET switch used to discharge the peak detector capacitor (100 pf). Clamp for the error voltage amplifier output is provided by the pair of reversed IN457 duo-diode groups. Timing waveforms are produced by mono-stable multivibrators.

The RCA CA3002 was originally selected because of its large gain control capability--up to 70 dB for a 1.5 V control voltage differential range. When the amplifier was tested to ascertain all of its operating characteristics, it was discovered that the maximum input voltage had to be limited to 150 mv p-p. Above this value, virtually independent of the gain control bias, the amplifier output exhibited a voltage saturation (compression) condition. The result was that the amplifier could not be driven to the levels intended in the original design. This, therefore, necessitated an adjustment of the intended operating point and resulted in a regulating range of 10 dB below the nominal input and 6.5 dB above the nominal input (rather than ± 20 dB). It was decided, however, that this would not compromise the prime reason for the breadboard evaluation of demonstrating excellent peak-to-peak regulation as a function of a variety of complex waveforms plus 4.5 MHz lowpass noise.

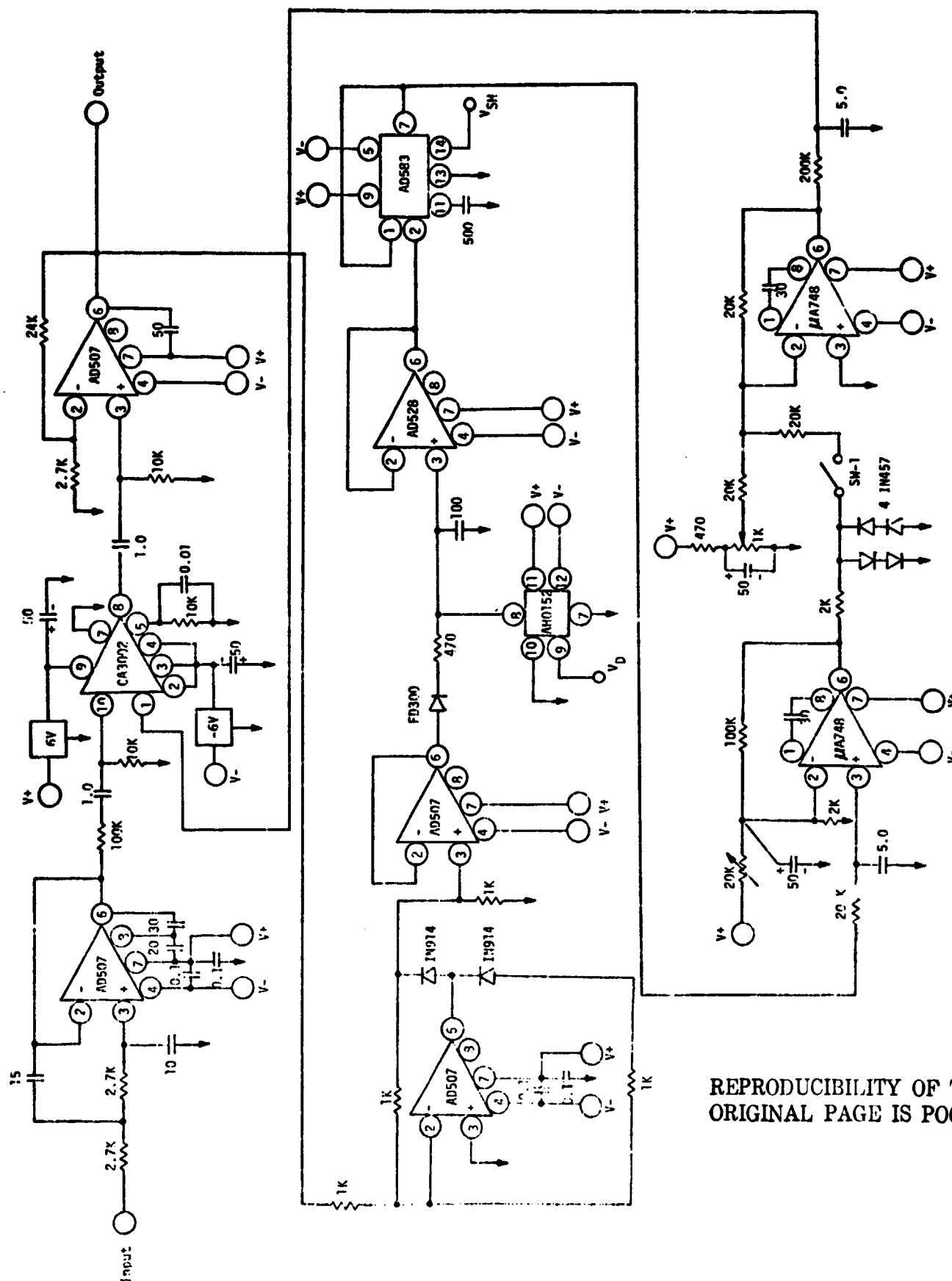


Figure 4.16. Peak Regulator Circuit Diagram

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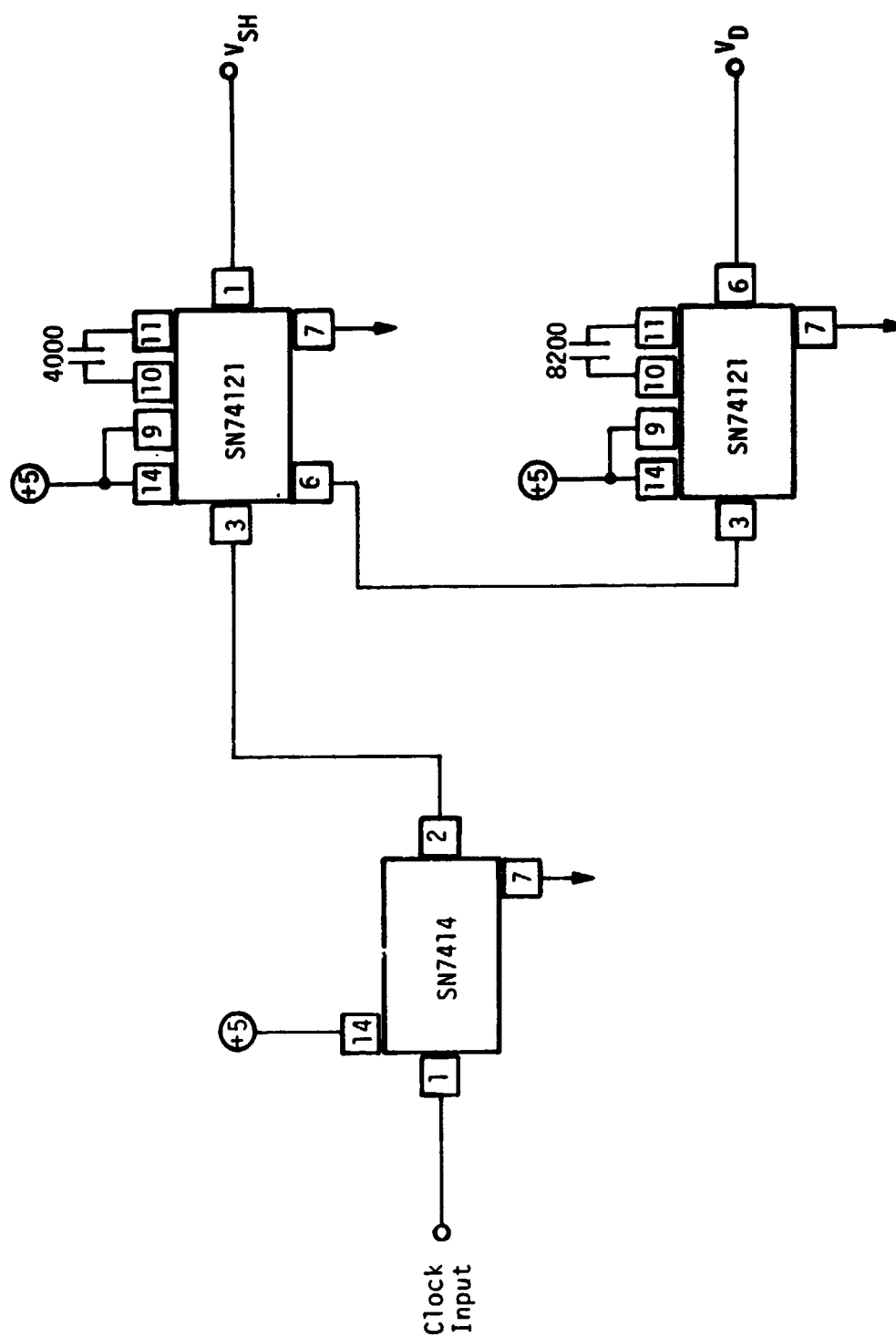


Figure 4.17. Peak Regulator Timing Logic Diagram

The initial regulator breadboard was constructed with a full wave linear rectifier. This circuit performed very well as a function of input frequencies up to 2.5 MHz. Above 2.5 MHz, however, unsymmetrical phase shifts appeared between the waveforms produced by the individual half-wave rectifier outputs. Further, the overall frequency response was limited to about 3 MHz due to the inability of the AD507 amplifiers to preserve the harmonic structure of the full-wave waveform above this frequency. Rather than redesign the full-wave rectifier using different (wider bandwidth) amplifiers, it was decided to use a linear half-wave circuit instead, as all the contemplated input waveforms are amplitude symmetrical. This change eliminated two AD507 amplifiers, with the result that the half-wave rectifier response was found to be adequate up to 4.2 MHz utilizing IN914 diodes.

All the remaining circuits performed essentially as expected. The peak error sampling rate was chosen as 1 kHz, and the peak detector averaging time per sample is 0.99 ms. Thus, for any of the various waveform shapes considered, where the lowest subcarrier (sinusoid) frequency is expected to be about 30 kHz and random noise occupies the full 4.5 MHz bandwidth, each peak sample should be very close to the true peak value of the waveform. Averaging over a thousand or so error samples also provides the loop with a reasonable rapid response to dynamic input level changes, but is sufficiently long to obviate response to very short signal transients or the possibility of an occasional impulse noise burst.

Table 4.26 summarizes the regulator performance measurements. As can be seen, the regulation range of -10 dB to +6.5 dB about the nominal (calibration) point was achieved.

The throughput frequency response of the regulator was measured exclusive of the LPF, and the 3 dB frequency was found to be about 5.2 MHz, the main contributor to the roll-off being attributed to the +20 dB output amplifier. With the input LPF connected, the throughput 3 dB frequency was 3.9 MHz.

The remainder of the measurements made on the regulator were rather qualitative and consisted of mixtures of signal waveforms and noise. A 1.024 MHz sine wave (representative of a subcarrier), a 200 kHz square wave (representative of NRZ data), and random noise were combined at varying levels and the regulator input and output observed on the scope. The

Table 4.26. Measured Peak Regulator Performance

V_i	V_o	% Error	
25	860	4.0	} Exceeds Regulator Specification
50	970	3.0	
100	992	0.8	
100	996	0.4	} Calibration
178	1000	0.0	
300	1002	0.2	
400	1006	0.6	
500	1009	0.9	
600	1011	1.1	} Exceeds Regulator Specification
700	1018	1.8	
800	1028	2.8	
900	1050	5.0	} CA3002 Amplifier in Compression
1000	1100	10.0	

All voltages are in mV-peak

performance was judged to be as expected. It was estimated that the regulator was able to hold regulation on the 4.5 MHz noise peaks at about 2.75σ .

The regulator was never observed to exhibit instability, and was able to accommodate input on/off step transients.

Except for the somewhat limited regulator dynamic range of 16.5 dB, all other aspects of the peak regulator design and breadboard evaluation met the objectives set for the effort. If, in the future, it is desired to increase the dynamic range to the original design goal of 40 dB, this may be done by replacing the CA3002 amplifier with a FET or diode current controlled attenuator configuration.

5.0 CONCLUSIONS

This report has covered Axiomatix's involvement and assessments with the evolving S-band hardware at TRW. The LRU's covered have been:

- (1) Network Transponder
- (2) Network Signal Processor
- (3) FM Transmitter
- (4) FM Signal Processor
- (5) Payload Interrogator
- (6) Payload Signal Processor.

The first four LRU's, which collectively represent the network hardware, have all passed through the qualification testing phase of development. As a result, Axiomatix's future involvement with these units will likely be limited to their performance as derived from system tests and any malfunction problems that might be attributable to basic design flaws.

Items (5) and (6), the payload PI and PSP units, have both passed through the preliminary design phase, but await critical design evaluations. (The CDR's are presently scheduled for April 1980.) As indicated in Sections 3.0, 4.1 and 4.2, there exists a number of open design and performance issues on these LRU's. Thus, Axiomatix will continue to monitor their development progress and provide supporting analysis with regard to design and performance for at least another year.

Other work has involved evaluation of the network transponder QTP and the ESTL network equipment verification plans. The QTP review has been completed. More activity, however, is planned with regard to the ESTL procedures as the work to date has only classified the tests in matrix form--it has not evaluated the test configurations in detail nor analyzed the data already produced from some testing.

REFERENCES

1. "Shuttle Orbiter S-Band Communications Equipment Design Evaluation," Final Report for Contract NAS 9-15514A, Axiomatix Report No. R7901-3, January 20, 1979.
2. "Shuttle Payload S-Band Communications Study," Final Report for Contract NAS 9-15240D, Axiomatix Report No. R7903-1, March 9, 1979.
3. Gardner, F.M., Phaselock Techniques, John Wiley & Sons, Inc, 1966.

APPENDIX A

DESCRIPTIONS OF THE PRINCIPAL AVIONIC EQUIPMENT

1.0 ORBITER AND PAYLOAD COMMUNICATION SYSTEM OVERVIEW

Figure A.1 is an overall interconnection diagram showing the Shuttle Orbiter principal communication hardware LRU's as well as the functional payload subsystems. The following sections describe at a functional detail level those Orbiter LRU's with which this contract has been concerned. Descriptions for the Payload Interrogator and the Payload Signal Processor are found in the main body of this report, subsections 4.1.1 and 4.1.2, respectively.

2.0 S-BAND NETWORK TRANSPONDER

A functional network transponder block diagram is shown in Figure A.2. The received signal, processed through the preamplifier in the TDRS mode or through the transponder triplexer receiver filter (high or low) in the SGLS or STDN direct link modes, is amplified by a low-noise S-band input amplifier prior to downconversion to approximately 240 MHz. A second coherent downconversion brings the signal to 31 MHz where, in the TDRS mode, despreading is accomplished by the spread spectrum processor which uses a noncoherent code search loop. The TDRS despread signal is routed to the carrier Costas loop used to derive phase tracking information. In the SGLS and STDN modes, the Costas loop configuration is also used to track the residual carrier. Demodulation of command and ranging signals is accomplished using an off-line wideband phase detector so that the Costas loop detector predetection bandwidth is optimized for tracking performance. Both tone ranging and data outputs from the receiver are noncoherently AGC'd to maintain a constant RMS signal-plus-noise level to the associated subsystems.

All frequencies are derived from two switchable VCXO subassemblies and one reference crystal oscillator. The reference oscillator operates at 31 MHz and thus places the second IF at 31 MHz. This is sufficiently high in frequency to provide good first IF image rejection and still allow the use of narrowband second IF filters. Channel selection

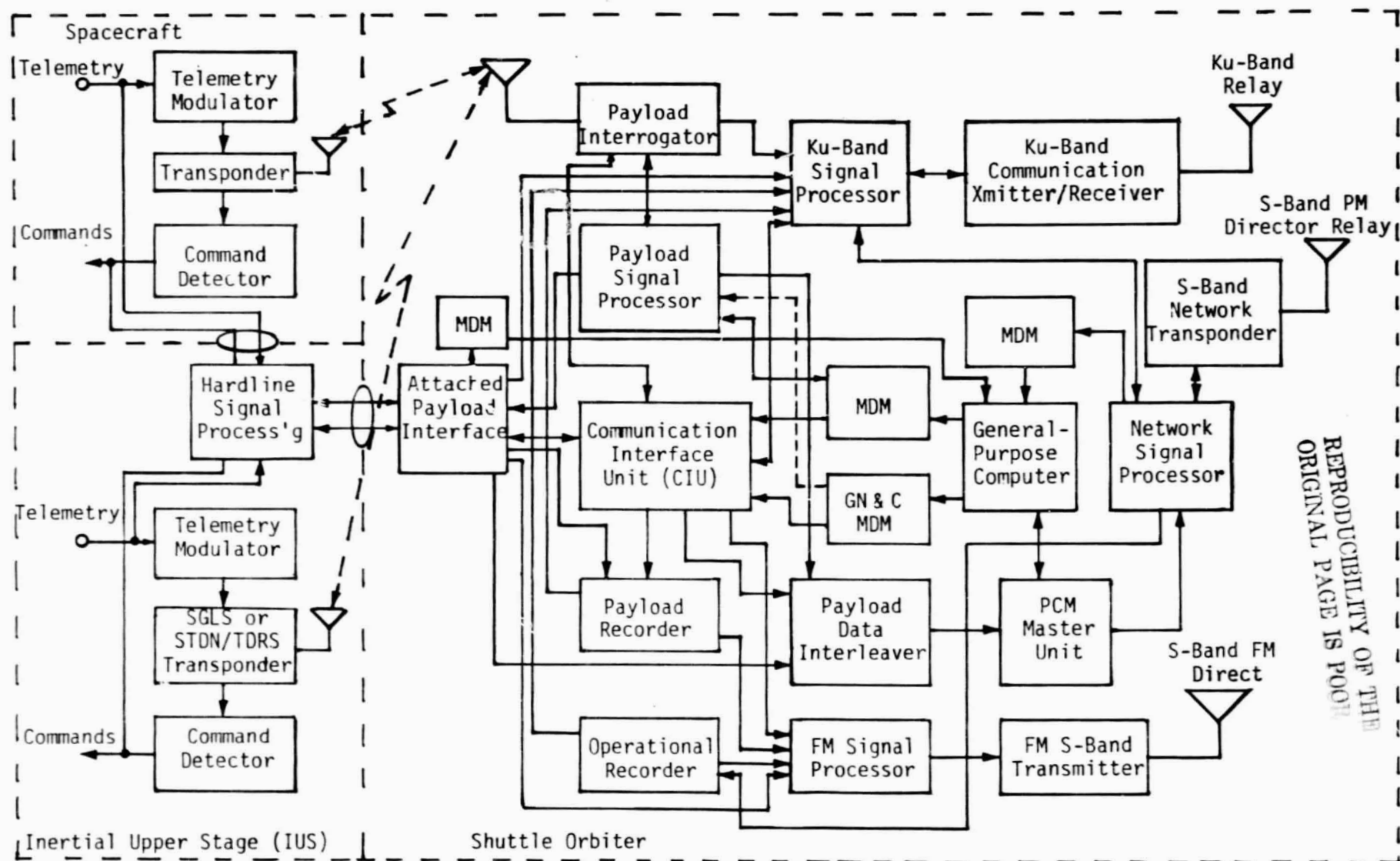


Figure A.1. Orbiter and Payload Communication Equipment and Configuration

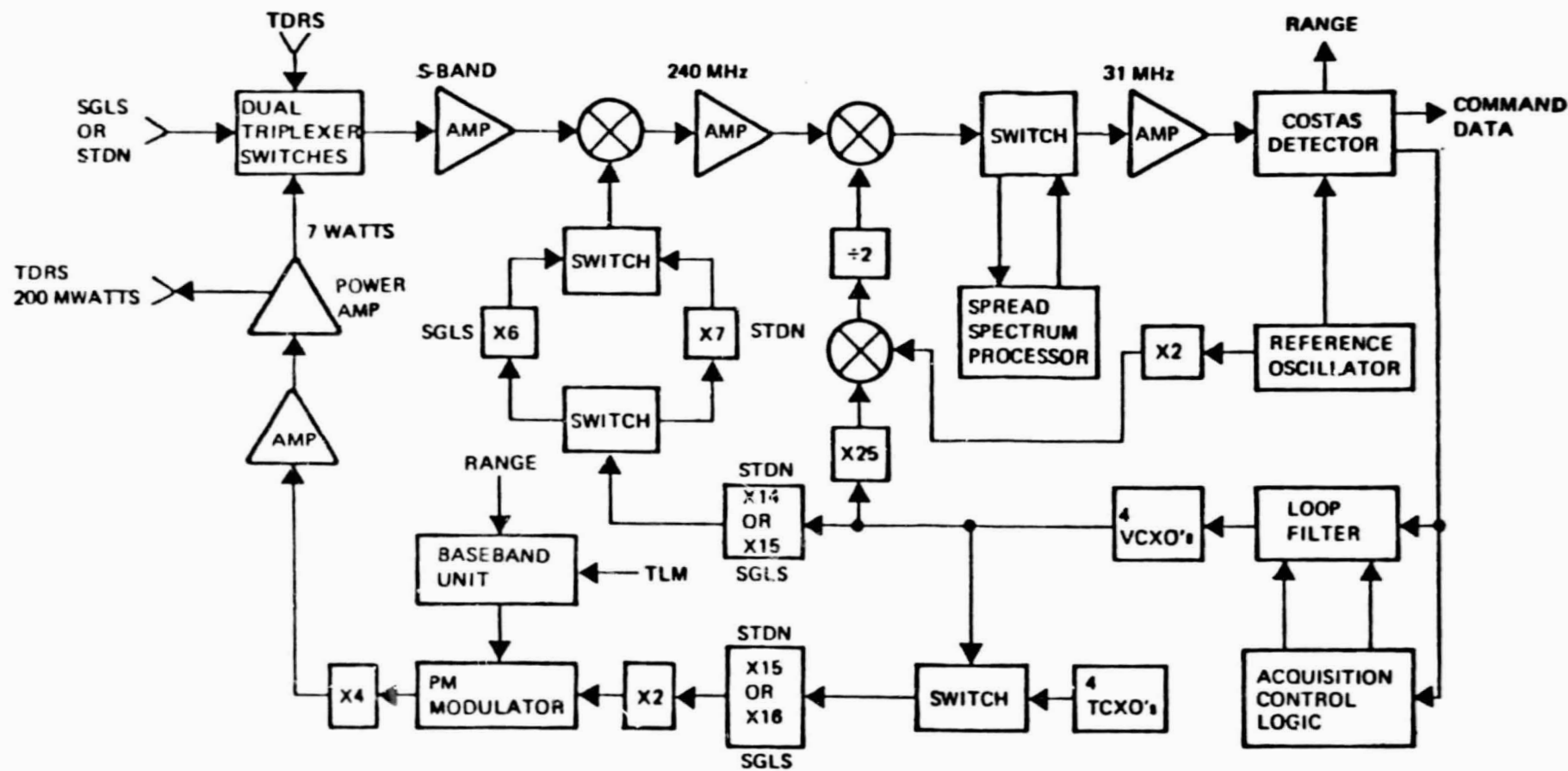


Figure A.2. S-Band Network Transponder Block Diagram

is provided by changing the VCXO frequency. Each VCXO subassembly contains four VCXO's for two-channel operation in either the SGLS or STDN/TDRS modes. A simple unique multiplier configuration is used, employing phase-locked oscillators to accomplish the x25 (second LO), x14 or x15 (first LO), and x15 or x16 (transmitter drive) multiplication. By simply changing the divider feedback ratios, the multiplication factor can be changed. This technique provides the wide percentage bandwidth multiplication required for multimode operation while yielding very low spurious products. The final first local oscillator multiplication ratio x6 or x7) is selected as a function of mode.

The third mixer in the second LO chain offsets the second LO frequency using a 62 MHz reference signal so that the second IF is fixed and does not vary as a function of received frequency. Therefore, the spread spectrum processor and the Costas loop preselection filters operate at the same frequency regardless of input channel selection. The drive frequencies to the third mixer are at twice the first IF and twice the reference oscillator frequency. This eliminates the potential problem of generating a high-level signal at the third mixer exactly equal to the first IF frequency, which could result in a self-lock condition.

Downlink STDN or SGLS linear modulation is accomplished at about 560 MHz, then multiplied by 4 to S-band. An S-band solid-state power amplifier provides a low-level (TDRS) or high-level (STDN/TDRS) output depending on mode selection.

3.0 NETWORK SIGNAL PROCESSOR (NSP)

The block diagram of the Network Signal Processor (NSP) is shown in Figure A.3.

The NSP consists of individual forward link return link, and record mode processing circuits. The three processes operate concurrently, thus providing full duplex operation of the forward and return links in addition to the record mode processing.

Mode controls define the particular data rates, the nature of the data, the need for convolutional encoding and decoding, and the need for voice delta modulating or demodulating. Interface controls define the input data source and the PCM telemetry source.

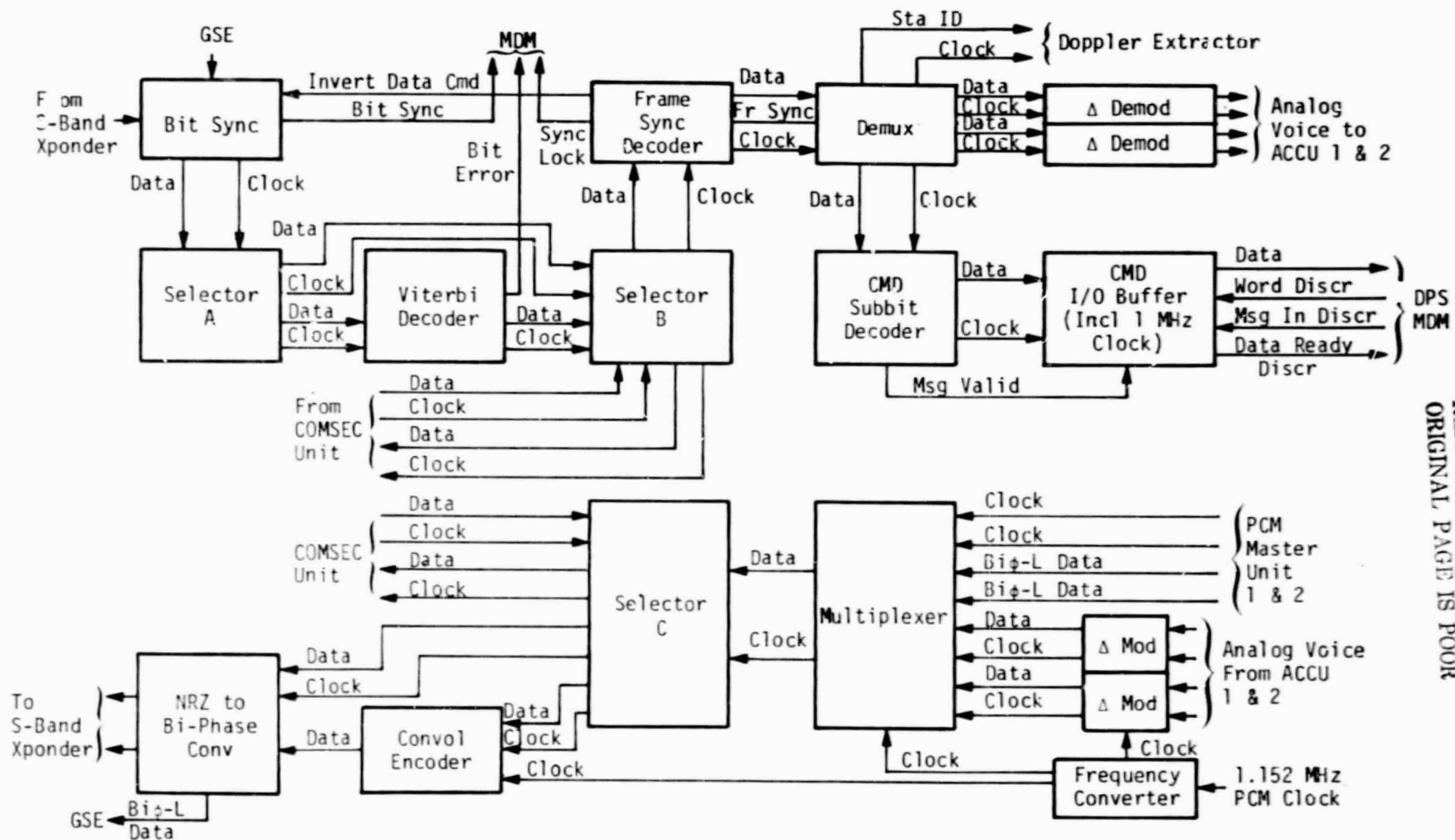


Figure A.3. Network Signal Processor Functional Diagram

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All input data is introduced through the bit synchronizer, with four input controls identifying the data source, one input control identifying the data rate, and another input control identifying the hard or soft decision. When bit synchronization is achieved, a status bit is provided to the MDM.

The bit synchronization data output and the derived clock are delivered to the convolutional decoder through selector A which has data invert control logic. Selector A is where the mode control determines if the convolutional decoder is to be employed. In the coded mode, the convolutional decoder provides its own data inversion capability. At selector B, if the data is identified as DOD data by mode control, it is output to the COMSEC unit and clocked back into the NSP after decryption.

Following detection (and decoding), the data is presented to the frame synchronization logic for frame pattern recognition. Once frame synchronization lock has been achieved, a lock signal informs the MDM of the frame synchronization status. Finally, the forward link function of demultiplexing and rate buffering is performed.

Command data is checked for errors in the BCH decoder, modified appropriately, and stored in a buffer. A message-valid pulse is sent to the MDM for every command word that passes the BCH and vehicle address checks. After 10 commands have been received, a signal is sent to the MDM indicating a data-present status. Upon request, 32 16-bit words are sent to an associated subsystem. The first word contains the status of the NSP, words 2 through 31 contain commands, and word 32 contains a bit for each command transmitted, representing the validity of that command.

The return link consists of multiplexing telemetry and voice data. The multiplexing function is keyed to the frame synchronization pattern included with the telemetry data. For DOD data, once the multiplexing function has been performed, the data is routed to the COMSEC equipment for encryption. All data (NASA or DOD) may also be convolutionally encoded as desired. Finally, the coded or uncoded data is NRZ-to-Manchester converted prior to transmission. Return link data is provided simultaneously to the S-band and Ku-band network.

The record mode multiplexes the voice data only with the selected 138 kbps PCM data. In NASA submode 1, the 128 kbps telemetry is multiplexed with the two dedicated voice channels. In NASA submode 2,

the 128 kbps telemetry is simply routed to the drivers for transmission to the recorders. In the DOD mode, the recorder data is taken from the return link COMSEC encrypter (effectively bypassing the entire record mode processing logic).

4.0 FM SYSTEM

Figure A.4 shows the diagram of the FM Signal Processor (FMSP) and Transmitter. The functions of baseband modulation, mixing, routing, impedance matching, and operational switching are accomplished by the signal processor. Payload signals, whether they be wideband analog, high-rate digital, or low-rate digital, are buffered in a matching network and passed through the mode selection and wideband amplifier to the FM transmitter.

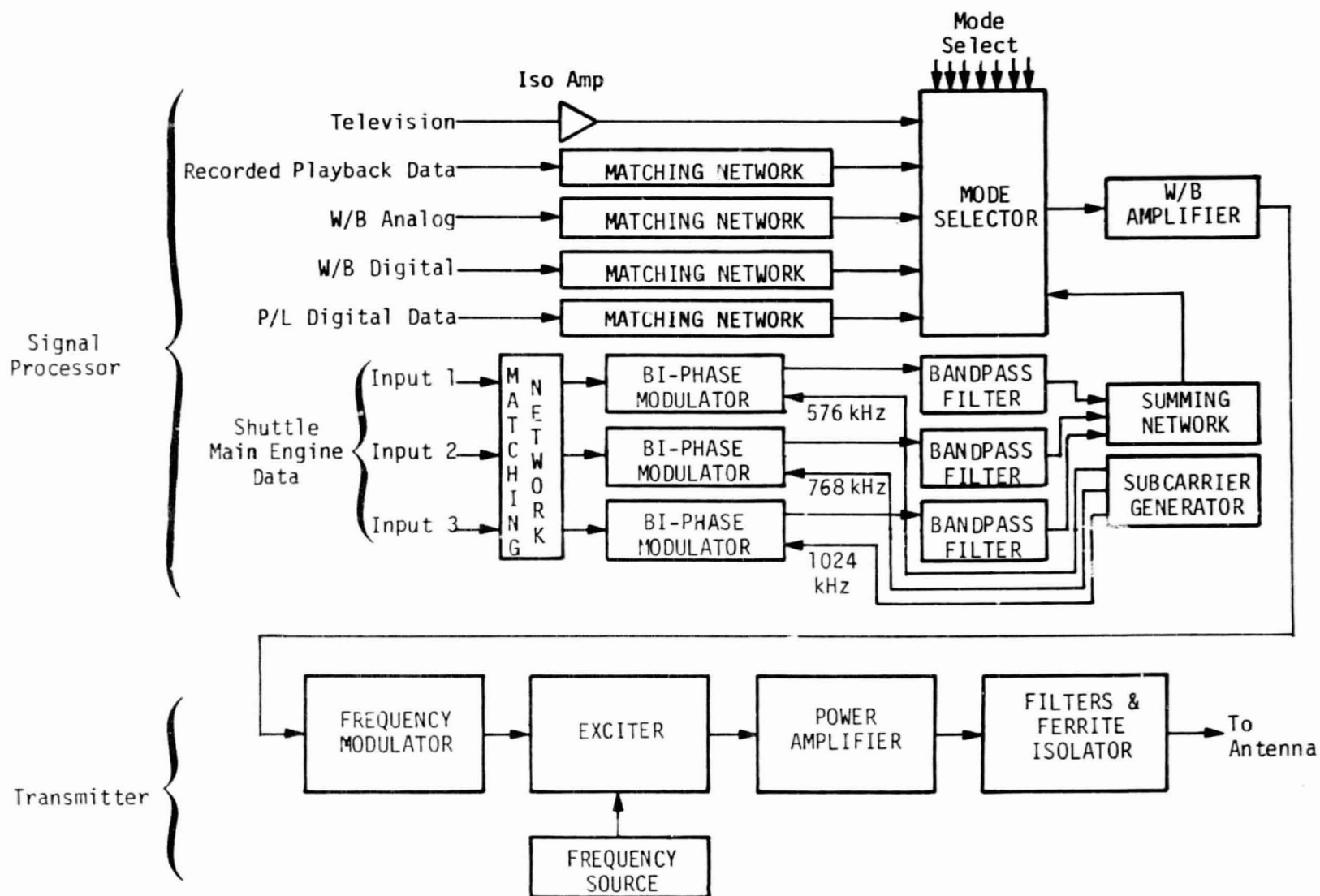
The FMSP and FM transmitter provide a capability for transmission of data not amenable for incorporation into the limited-rate PCM telemetry data stream. The data to be transmitted via FM include television, digital data from the main engines during launch, wideband payload data, or digital data from the PR or the API. Video and wideband digital and analog signals are routed to the FM transmitter with only matching and filtering, but narrowband digital engine data are placed on subcarriers at 576, 768 and 1024 kHz. No pre-emphasis or other special processing is employed.

The FM transmitter provides the functions of carrier frequency modulation and RF power amplification. It operates at 2250 MHz with an output power of 10 W. Both baseband and RF filtering are provided to reduce out-of-channel interference to the Network Transponder, PI, and payload receivers. The nominal RF bandwidth is 10 MHz.

4.1 Ku-Band Signal Processor (KuSP)

The Ku-Band Signal Processor (KuSP) shown in Figure A.5 performs the functions of data and signal processing for the Ku-band forward and return links. For the forward link, two modes are available:

- (1) A special mode for amplification and impedance matching of data from the Ku-band receiver and communication processor assemblies for delivery to the NSP.



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Figure A.4. FM Processor and Transmitter

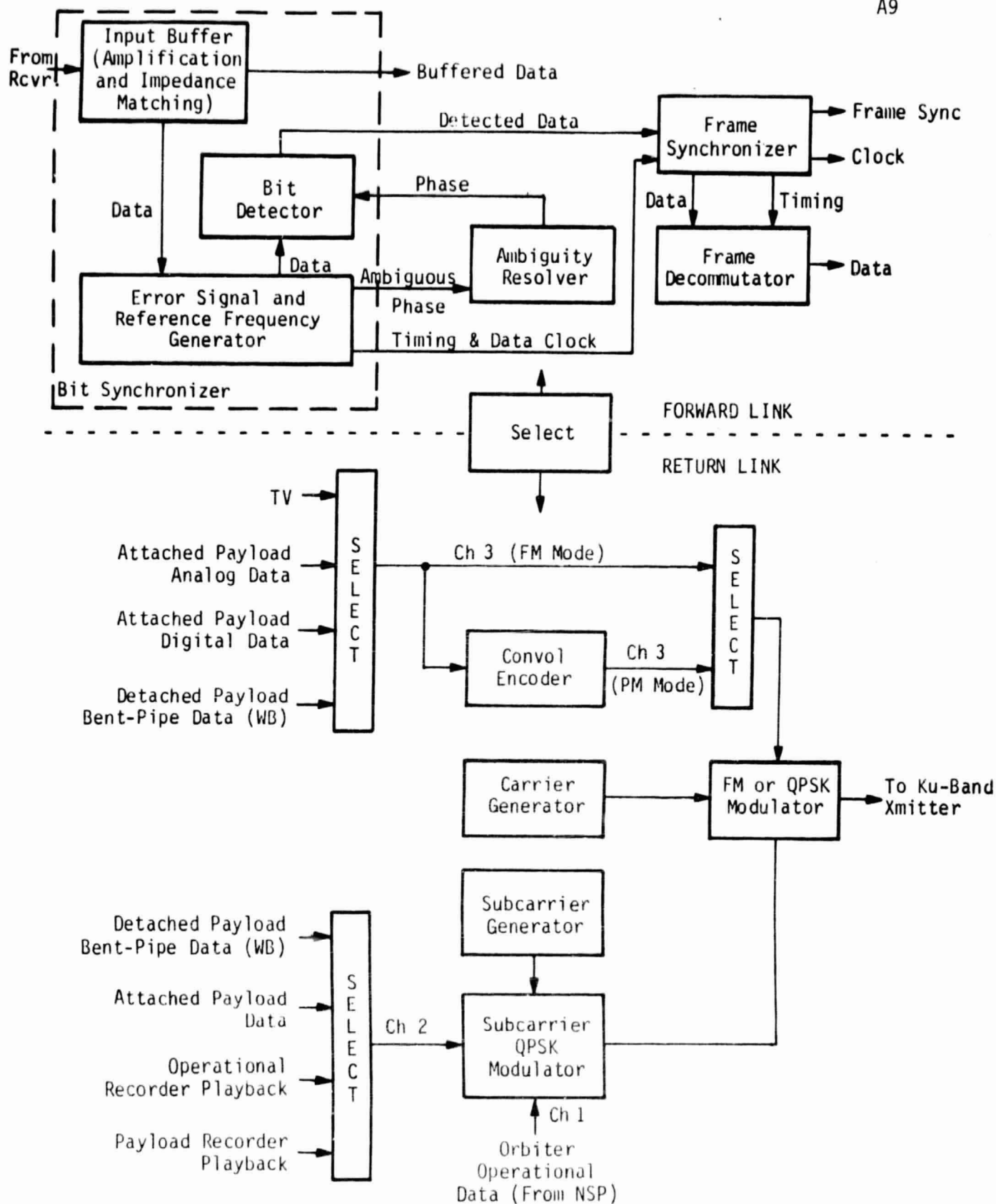


Figure A.5. Ku-Band Signal Processor Block Diagram

(2) A normal mode which performs the operations of bit synchronization, clock generation, ambiguity resolution (data and clock), bit detection, frame synchronization, and data decommutation of Ku-band received data.

Return link signals are handled in the KuSP by modulating the data in one of two modes before up-conversion to Ku-band frequencies. The two selectable modes multiplex three channels carrying a wide variety of data. In mode 1, the PM mode, the high-rate data channel is convolutionally encoded before modulation onto the carrier. The lower rate data channels 1 and 2 are QPSK modulated onto a square-wave subcarrier which is, in turn, PSK modulated in quadrature with channel 3 onto the carrier.

6.0 PAYLOAD DATA INTERLEAVER (PDI)

A block diagram of the Payload Data Interleaver (PDI) is shown in Figure A.6. It is basically a multiplexer capable of combining various asynchronous data streams into a single serial data stream. The PDI provides for reception of up to six asynchronous payload PCM streams, five from attached payloads and one from the PSP that is active (detached payload). An input switch matrix selects four of the inputs for the bit synchronizers. The "chain" functions of bit synchronization, decommutation and word selection are provided for up to four simultaneous PCM streams in two possible modes:

Mode 1: In this mode, a chain bit synchronizes, master-frame synchronizes, minor-frame synchronizes, and word synchronizes to the incoming data stream. The word selector blocks data into proper words for storage in the data RAM and/or toggle buffer. PCM code type, bit rate, PCM format, synchronization codes, and word selection are programmable under control of the decommutator format memories. Two word selection capabilities for this mode of operation are as follows:

Type I: The first type selects all, or a subset of, the words in a payload PCM format minor frame (or master frame for formats without minor frames) for storage in the toggle buffer.

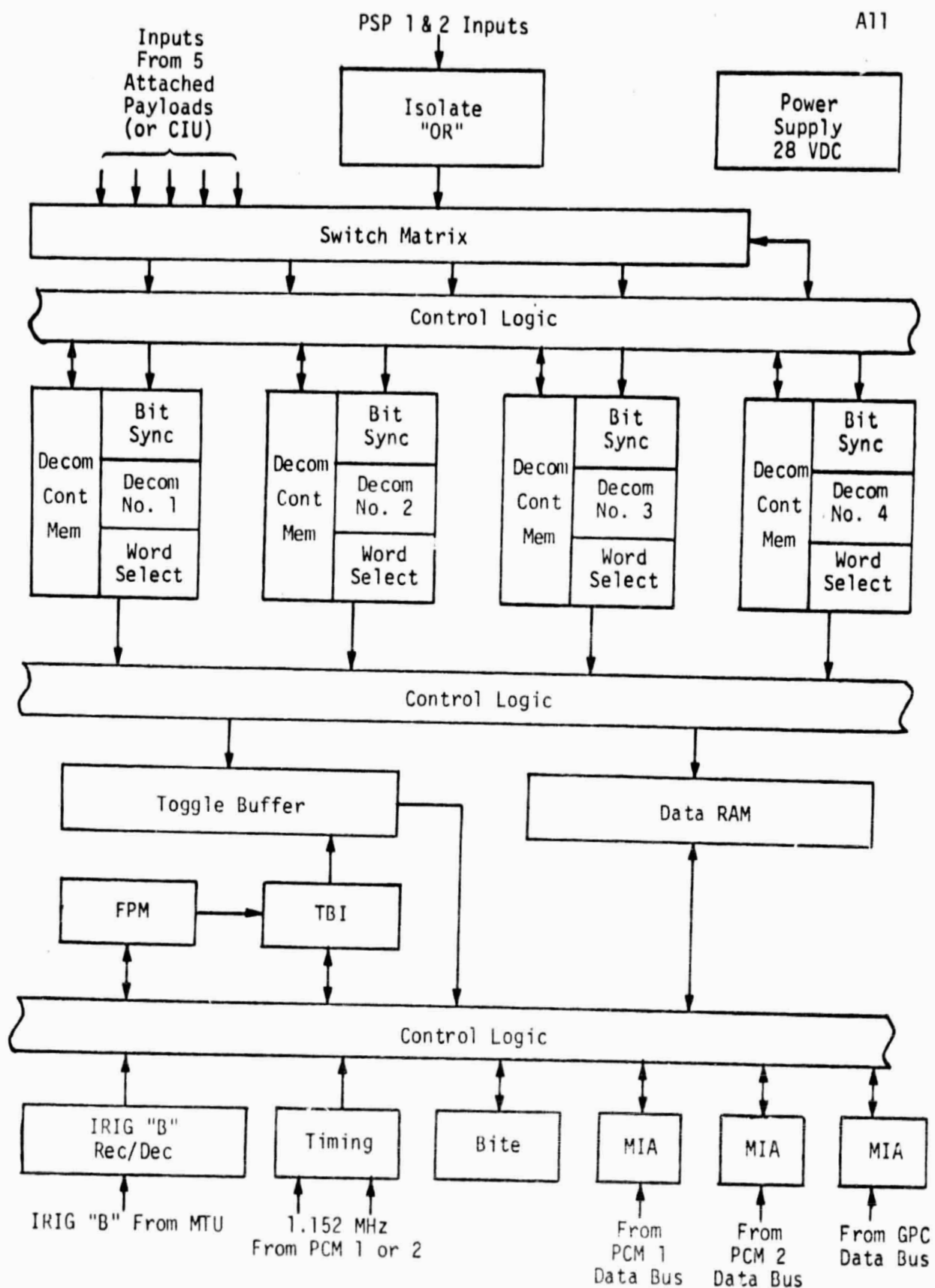


Figure A.6. PDI Block Diagram

Type II: The second type of word selection is by parameter. The specification of a parameter consists of its word location within a minor frame, the first minor frame in which it appears, and its sample rate. The specification is provided as part of the decommutator control memory format load.

Mode 2: In this mode, a chain bit synchronizes to the incoming data, blocks it into 8-bit words, blocks the 8-bit words into frames, supplies synchronization pattern at the start of each frame, and includes the status register as the last three 16-bit words of each frame. A homogeneous data set for this mode of operation is defined as all information within this PDI-created frame. Code type, bit rate, frame length, and synchronization pattern are programmable under control of the decommutator format memories. The frames are supplied to the toggle buffer for storage as homogeneous data sets. No data is supplied to the data RAM in this mode of operation.

A status register containing the status and time for a given chain operation is provided by the word selector to the Toggle Buffer (TB) control logic. This logic regulates access to and from the half buffers by the word selectors and the data buses. All requests for TB data by the data bus ports are processed through the Fetch Pointer Memory (FPM) and the Toggle Buffer Identifier (TBI). The TB control logic also partitions data from the word selector into homogeneous data sets for access by the data bus ports.

The FPM is used to identify which TB is to be accessed by a data bus port. It also allows access to any location in the data RAM by any of the PDI data bus ports at any time. FPM control logic routes all requests for TB data to the location in the FPM identified by the data bus command word. It further provides for loading and reading of formats to and from the FPM at any time by the data bus ports.

A data RAM for storage of data from the word selector by parameter is provided. The data RAM control logic steers data provided by the word selector into addresses in the data RAM specified by the decommutator control memory.

There are three data bus ports for interface with the Orbiter GPC that have read and write access into the switch matrix, the decommutator control memory, the FPM, the PDI, and the data RAM.

An IRIG "B" receiver/decoder accepts an IRIG "B" code from an external source, decodes time, and supplies it to the four status registers.

7.0 MULTIPLEXER/DEMULTIPLEXER (MDM)

The primary interface unit between the GPC and other subsystems is an MDM, shown in Figure A.7. The MDM's act as a GPC-to-Orbiter format conversion unit. They accept serial digital information from the GPC's and convert or format this information into analog, discrete or serial digital form for transfer to Space Shuttle subsystems. The MDM's can also receive analog, discrete or serial digital information from the Space Shuttle subsystems and convert and format these data into serial digital words for transfer to the GPC. In addition, MDM's are used by the instrumentation subsystems, but only in a receive mode. Each MDM is controlled through either the primary port connected to the primary serial data bus or through the secondary port connected to the back-up serial bus if failure is encountered with the primary system. The input and output of the MDM are via a multiplexer interface adapter (MIA). When the Word Discrete is switched to a logical "1" state, the Orbiter subsystem is enabled to transmit individual words to the MDM. The burst data rate to the MDM is 1 Mbps, and the first three bits of each MDM word are used for word synchronization and are different from the normal Manchester-coded bits. When the Message Discrete is switched to a logical "1" state, the Orbiter subsystem is initiated to transfer multiple words under the control of the Word Discrete, beginning with the first word.

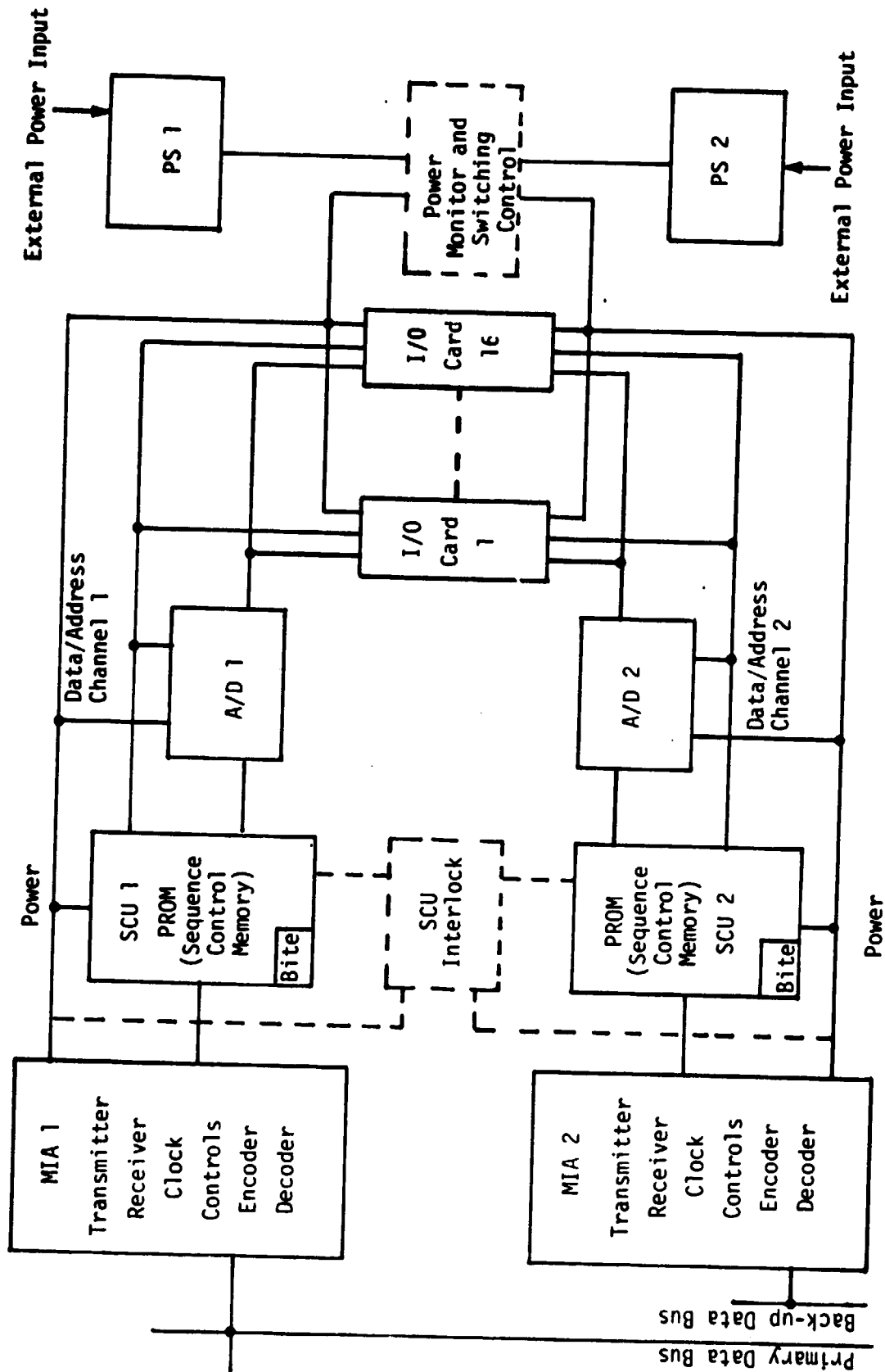


Figure A.7. MDM System Block Diagram

APPENDIX B

PROCEDURE TO CALIBRATE THE SHUTTLE LRU TEST SET
COMMERICAL BIT SYNCH AGAINST THE EM NSP BIT SYNCH.

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CODE IDENT 11982

TITLE

PROCEDURE TO CALIBRATE THE SHUTTLE
LRU TEST SET COMMERCIAL BIT SYNCH
AGAINST THE EM NSP BIT SYNCH.

DATE JUNE 22, 1978

NO. WR-06H-20A

SUPERSEDING: WR-06H-20
MAY 15, 1978

REFERENCE PRINT
CONFIGURATION & DATA MANAGEMENT
ISSUED

JUN 14 1979

WILL NOT BE MAINTAINED CURRENT

PREPARED BY: W. R. Hook
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APPROVAL SIGNATURES:

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DATE

720000 7/6/78
DATE

DATE

DATE

1. OBJECT

The general object of this procedure is to calibrate the LRU test set commercial bit synchronizer against the EM NSP bit synchronizer in order to allow a meaningful evaluation of the absolute BER performance of the flight transponder when tested with the LRU test set. The specific information which can be obtained from this calibration data includes:

- Verification that the flight transponders will perform approximately the same as the EM transponder when operated with the EM NSP.
- Verification that there are no anomalous and/or catastrophic BER degradations which will not be detected using the (primary) functional test procedure pass/fail degradation criteria and test method.

This calibration data is not to be used in the calculation of the (RI specified) transponder degradation performance. Rather it is to be used to carry out an independent cross-check which will increase confidence that the BER performance of the flight transponder, when operated with flight NSP's, will be as expected based on the results of the LRU tests. ~~THE accuracy of transponder BER degradation results which can be obtained using this calibration data is significantly poorer than that which can be obtained using the method outlined in the functional test procedure (FTP).~~ ~~THIS IS why the FTP method is used for primary sell-off.~~ Nevertheless, each transponder must pass the test outlined in this procedure, as well as pass the primary FTP test.

2. APPROACH

The general approach is to measure the performance of the EM transponder with the EM NSP bit sync using the subsystem test set at TRW Redondo Beach. Next, to ship the EM transponder to TRW CE Colorado Springs and to remeasure the same data using the commercial bit sync with the LRU Test Set. Finally, to ship the EM transponder back to TRW Redondo Beach and to confirm that the shipping process did not change performance. The specific steps include:

2.1 Measure the BER performance at 32 Kbps coded and 32 Kbps uncoded using the EM transponder and EM NSP; use the subsystem test set; obtain BER as a function of C/N_0 . (Typical curves are shown in Figure 2-1a and 2-1b). Verify that BER performance is comparable to previous measured results.

2.2 Ship EM transponder to TRW CE.

2.3 Measure the BER performance at 32 Kbps uncoded using the EM transponder and the commercial bit sync; use the LRU Test Set; obtain BER as a function of C/N_0 (see Figure 2-1c for typical result). The difference ("delta") between this curve and the uncoded curve obtained in Step 2.1 is the calibration factor which allows the prediction of the ultimate subsystem performance of flight units tested with the LRU test set. Notice that this difference "delta" includes the difference between the subsystem test set measurement of C/N_0 and the LRU test measurement of C/N_0 , as well as the intrinsic performance difference between the two bit syncs.

2.4 Measure the BER performance at 10.29 KBPS uncoded using the EM transponder and the commercial bit sync; use the LRU test set; obtain BER as a function of C/N_0 (see Figure 2-2a for typical result). This is the curve that allows a direct comparison of the flight transponder with the EM transponder, and is the basis for the secondary pass/fail criteria, which this procedure is designed to provide

2.5 Establish the flight transponder secondary pass/fail limit by adding 0.3 dB to the results of Step 2.4, as shown in Figure 2-2b. (The 0.3 dB includes an allowance for bit sync performance variation, plus an allowance for C/N_0 setting uncertainty).

2.6 Ship EM transponder to TRW Redondo Beach.

2.7 Repeat Step 2.1; verify that results are within 0.2 dB of Step 2.1.

Figure 2-1(a). Typical Results,
32 Kbps Coded,
with NSP

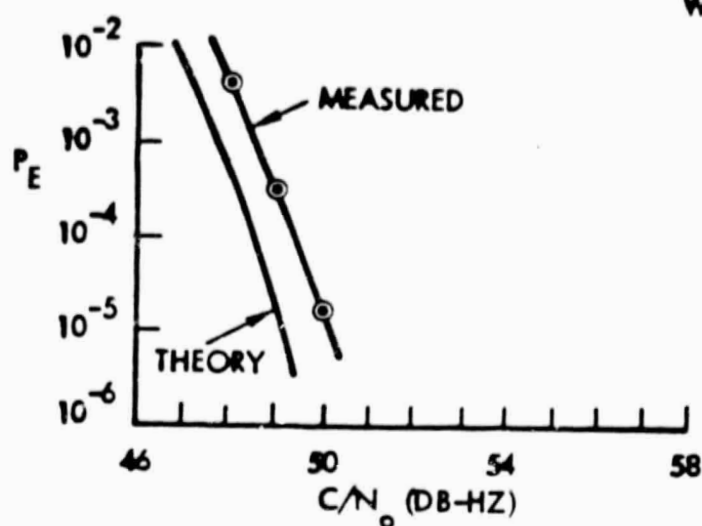


Figure 2-1(b). Typical Results,
32 Kbps Uncoded,
with NSP

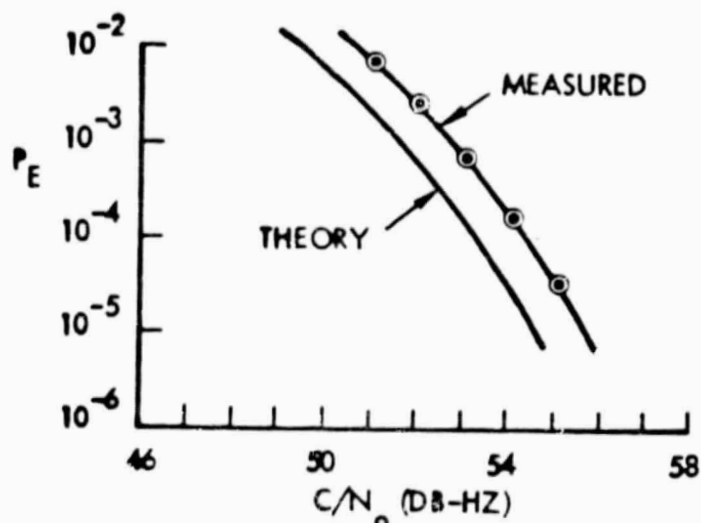
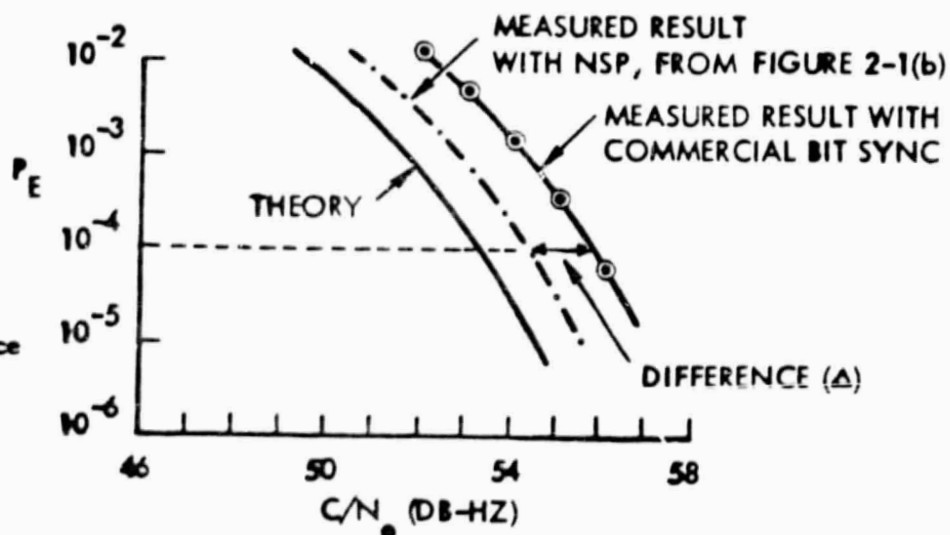


Figure 2-1(c). Typical Results,
32 Kbps Uncoded,
with Commercial
Bit Sync (Also
Shows the Difference
(Δ) Between it and
the NSP Results)



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Figure 2-2(a). Typical Results,
10.29 Kbps
Uncoded, with
Commercial Bit
Sync

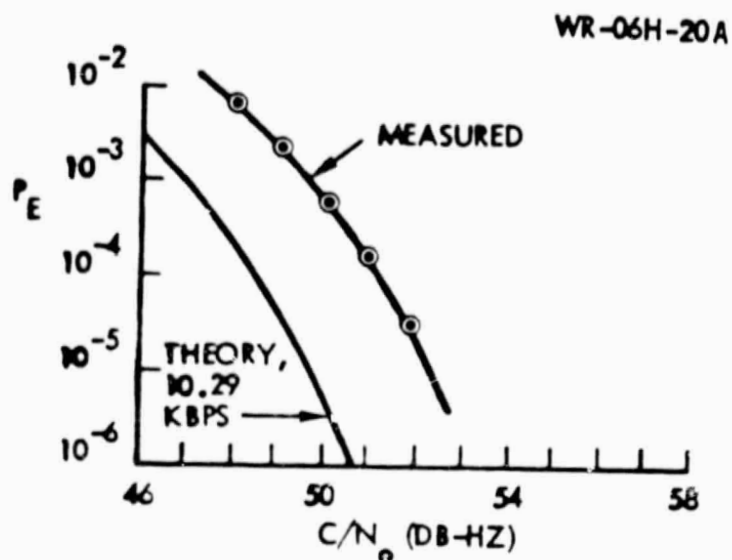


Figure 2-2(b). Secondary Pass/
Fail Limit Curve

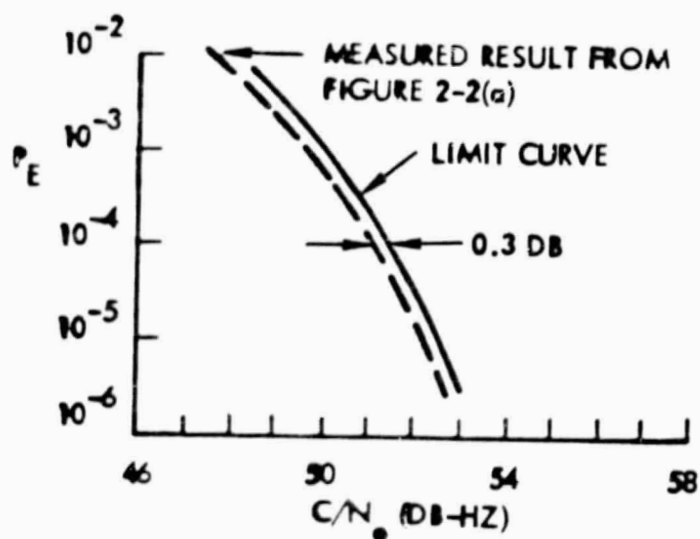


TABLE 1 -

S-Band Transponder
BER Test

P/N 292001

S/N

Date

INITIAL SWITCH POSITIONS: (1,1) (2,1) (3,1) (5,1) (6,1)
(13,1) (26,1) (138,1) (141,1) (142,1) DATA LO, TDRS

Tech

Config. No.	Switch Position Changes	Transponder		Input Signal			BER N	Test Results		Average BER	Limit Curve No.	Pass
		Prime Mode	Freq. Mode	Data Rate (Kbps)	Frequency (MHz)	C/N ₀ (dB)		Individual BER Counts				
31		TDRS	HI	10.29	2106.351	50.0	10 ⁵				REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR	
32		TDRS	HI	10.29	2106.351	51.0	10 ⁵					
33		TDRS	HI	10.29	2106.351	52.0	10 ⁶					
37		TDRS	HI	32.0	2106.351	55.0	10 ⁵					
38		TDRS	HI	32.0	2106.351	56.0	10 ⁵					
39		TDRS	HI	32.0	2106.351	57.0	10 ⁶					

- NOTES: 1. All configurations have doppler frequency shift of -55 kHz.
2. Configurations 17 to 36 have noise input of -151 dBm.

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Figure 4-1. MEASURED DATA

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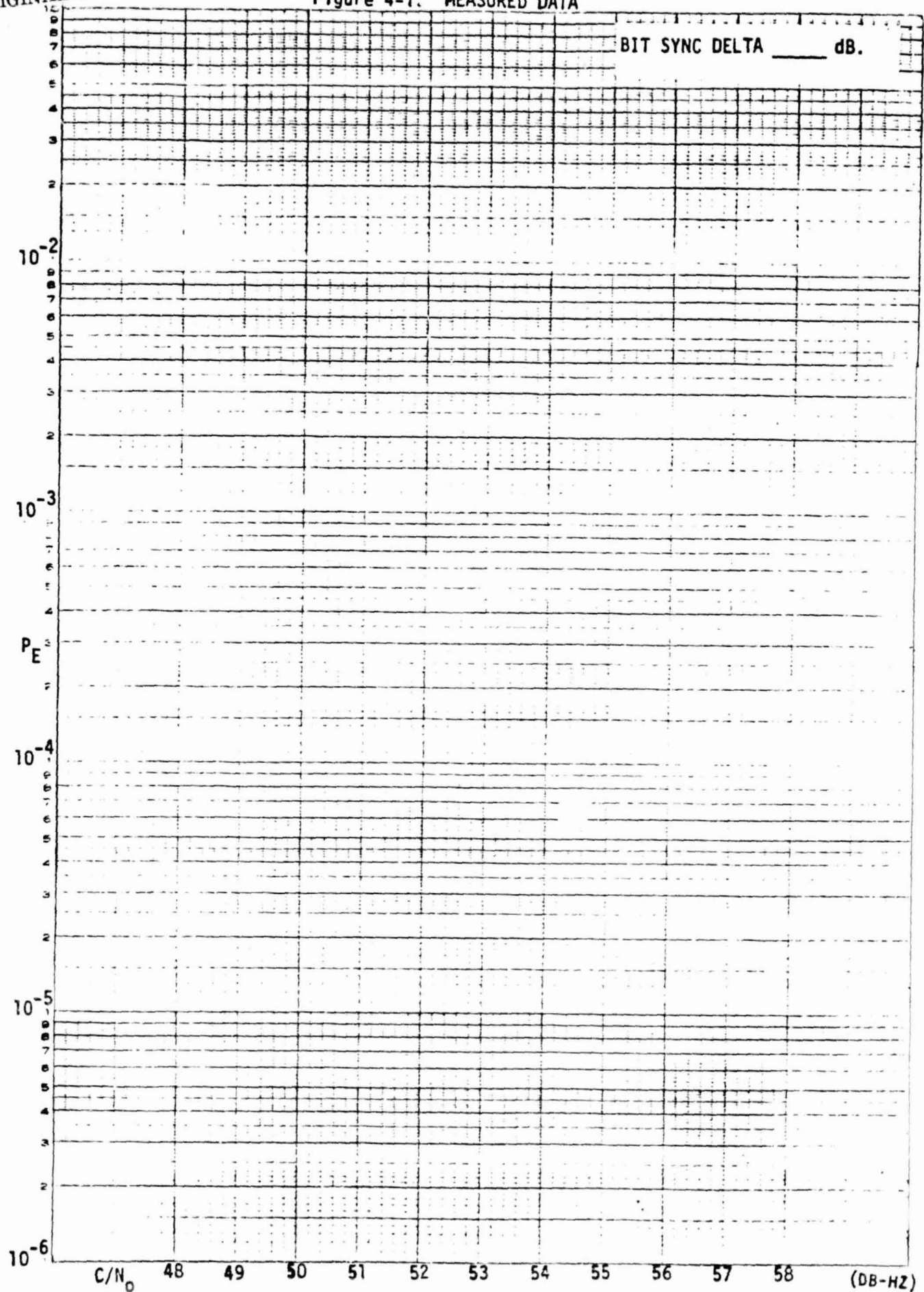
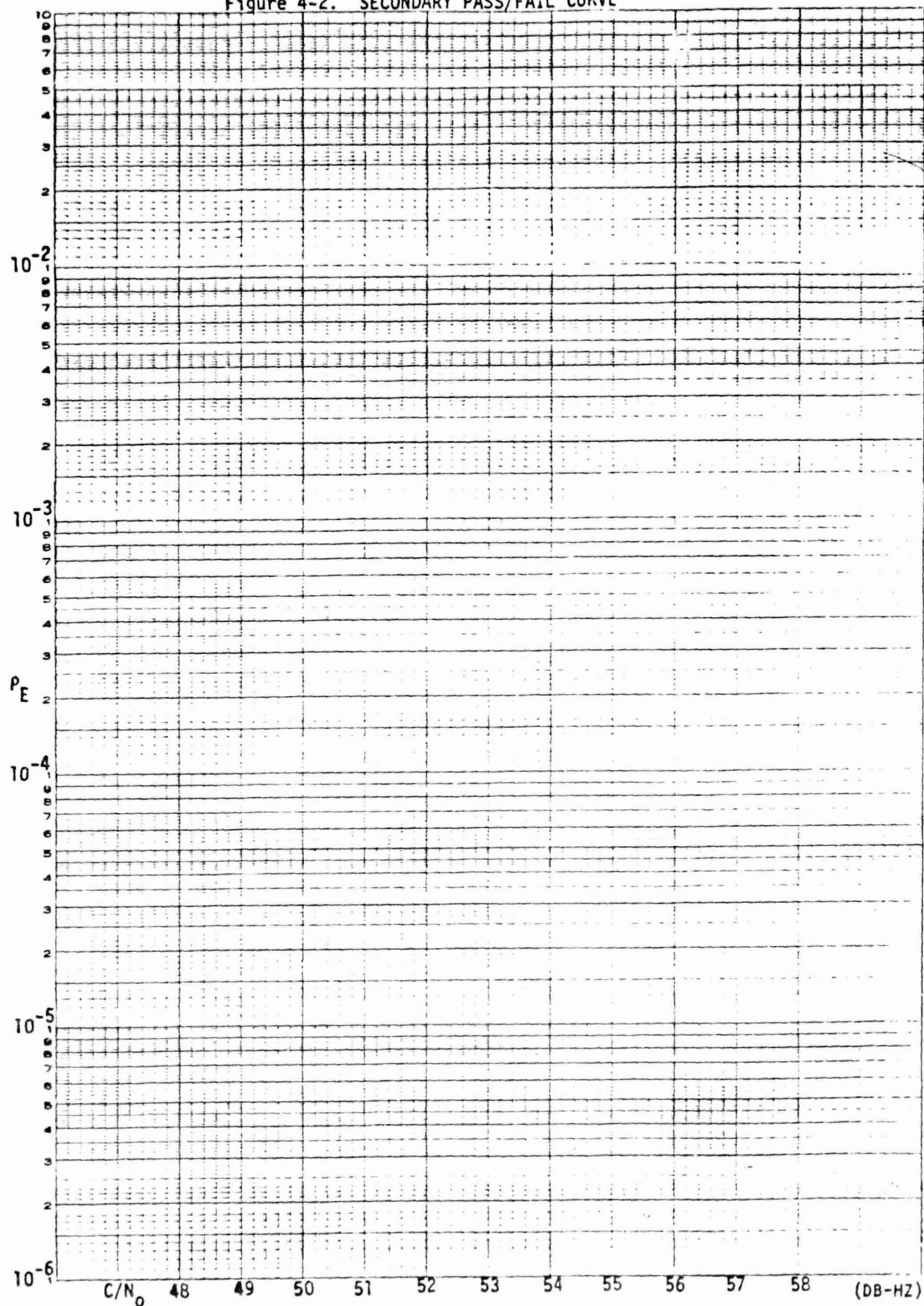


Figure 4-2. SECONDARY PASS/FAIL CURVE



APPENDIX A — MEASUREMENT OF C/N_0 USING THE SUBSYSTEM TEST SET

There are two C/N programs (C/NB and CNO); both programs have a different method of measuring C/N. It is understood that the ideal receiver is set up properly when the answers of both the programs (C/NB and CNO) agree within .06 dB. A brief description of the programs is contained below. Figure A1 is the test setup. The FORTRAN listings are also attached.

1. PROGRAM C/NB

- a) Measure noise level at D with A and B terminated and C in thru position.
- b) Set signal to same level at D as measured at D above with signal routed in thru directional coupler port via B, and C terminated.
- c) Add noise to above (b) signal by switching C to thru position with separate signal and noise now applied to the Ideal RX at coupler. Note level at D. (This should be 3.0 dB increase.)
- d) Add signal to noise at A and terminate B. Use "Power Set" program to set level noted at step (c) above.
- e) "Power Set" level in (d) above is level that carrier equals noise.

2.0 PROGRAM CNO

- a) Suppress signal at A and terminate B and C in thru position.
- b) Measure noise at D (note level).
- c) Using "Power Set" program increment signal until level is within .01 dB of the level measured in (b) above +3.00 dB. (Note Power set level.)
- d) Power set level in (c) above is carrier equal noise.

WR-06H-20 A

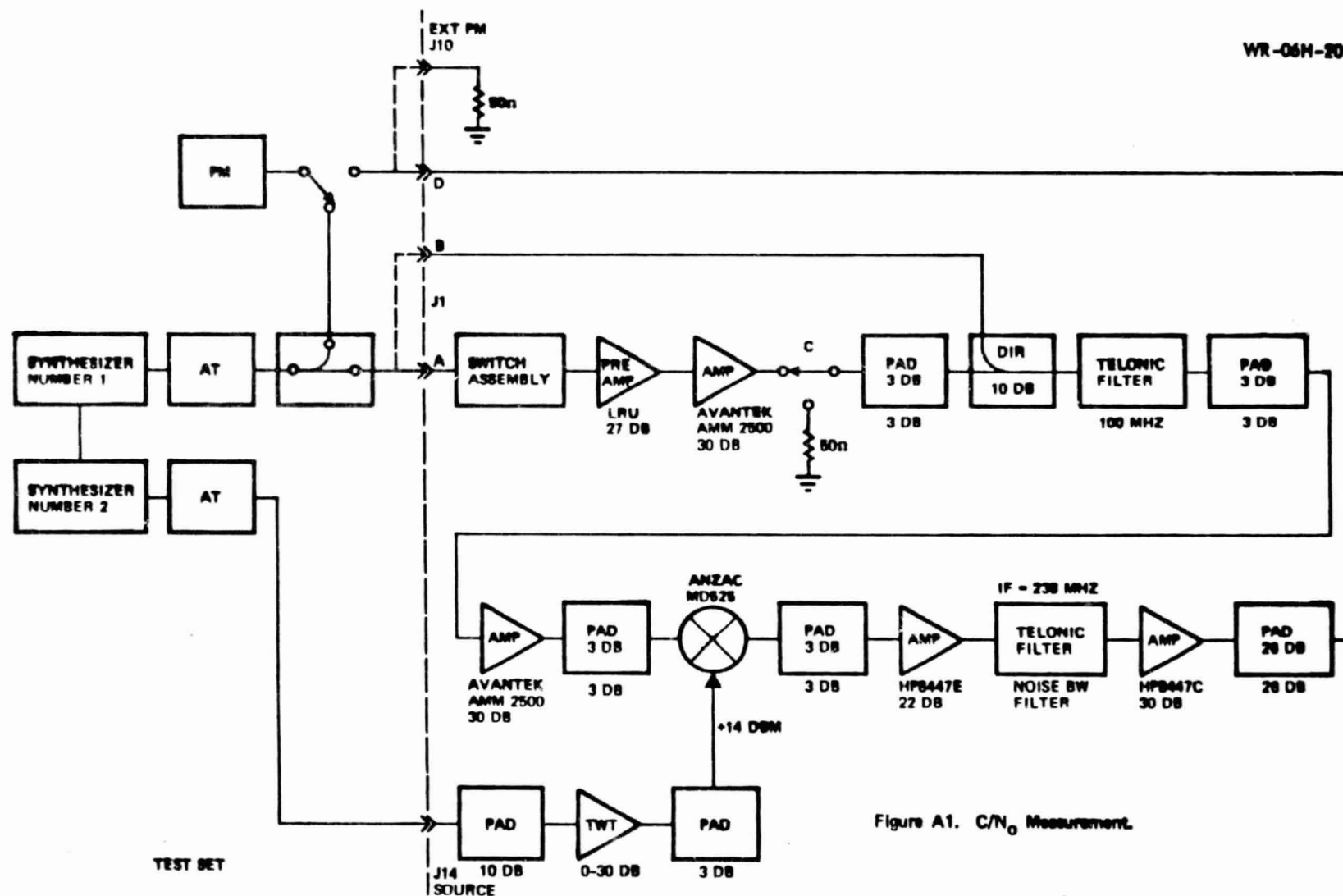


Figure A1. C/N₀ Measurement.

C/NB T=00004 IS ON CR00020 USING 00044 BLKS R=0016

```

0001 10REM                                C/NB TEST PROGRAM
0002 20REM                                *****
0003 30REM                                SIGNAL & NOISE MATCHING & SUMMING
0004 40REM
0005 50REM =====
0006 60REM GET PROGRAM TURN-ON PARAMETERS & INITIALIZE
0007 70REM -----
0008 80REM
0009 120REM P2 = UUT CONFIGURATION # FOR C/NB TEST - TEST SETUP BYPASS
0010 130REM      = NEGATIVE VALUE: CAUSES TEST SET SETUP BYPASS
0011 140REM      = 9999           : CAUSES UUT CONFIGURATION BYPASS
0012 150REM
0013 160REM P3 = <UNUSED>
0014 170REM
0015 180REM P4 = INPUT SIGNAL POWER FOR C/NB SETPOINT - TRUE VALUE IN DBM
0016 190REM      = 0 : UUT CONFIGURATION TABLE VALUE
0017 200REM
0018 240REM
0019 250LET P2=7001
0020 260LET P3=0
0021 270LET P4=0
0022 280REM
0023 290REM L9 = LU # FOR HARDCOPY OUTPUT
0024 300LET L9=6
0025 310REM L9 = LU # FOR DEBUG OUTPUT
0026 320LET L9=3
0027 330REM B = NOISE BANDWIDTH (DB)
0028 340LET B=0
0029 350REM R = INITIAL PWR RESET FOR FINAL C/N
0030 360LET R=-101
0031 370REM
0032 380REM
0033 390PRINT #L9;"TURNON PAPMS ";P2,P3,P4
0034 400REM
0035 410REM =====
0036 420REM TEST SET SETUP
0037 430REM -----
0038 440REM
0039 450IF (P2<0)GOTO 500
0040 460LET E1=SETUP(700)
0041 470IF (E1#0)GOTO 3440
0042 480REM
0043 490REM =====
0044 500REM UUT & INPUT SIGNALS CONFIGURATION
0045 510REM -----
0046 520REM
0047 530PRINT "C/N - PWR LEVEL CORRELATION"
0048 540PRINT #L8;" C/N - PWR LEVEL CORRELATION"
0049 550REM BASIC TIME-DATE CONVERSION & PRINTOUT
0050 560LET D9=TIM(2)
0051 570FOR M9=1TO 12
0052 580LET S9=31
0053 590IF (M9=2)LET S9=28
0054 600IF (M9=4OR M9=6OR M9=9OR M9=11)LET S9=30
0055 610IF (D9<= S9)GOTO 640
0056 620LET D9=D9-S9-
0057 630NEXT M9
0058 640PRINT #L8;" DATE =";M9;" / ";D9;" / ";TIM(3),"TIME =";TIM(1);";";TIM(0)

```

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0059 650PRINT "CONFIGURATION 0 =" ; P2
0060 660PRINT @L8;" CONFIGURATION 0 =" ; P2
0061 670PRINT
0062 680PRINT "TERMINATE POWER METER EXTERNAL PORT IN 50 OHMS"
00 690PAUSE
0064 700REM
0065 710IF (ABS(P2)=9999)GOTO 760
0066 720REM
0067 730LET E1=CF(ABS(P2))
0068 740IF (E1=0)GOTO 3440
0069 750REM
0070 760IF (ABS(P4)=0)GOTO 790
0071 770GOTO 970
0072 780REM
0073 790IF (ABS(P2)=9999)GOTO 830
0074 800LET E1=-901
0075 810GOTO 3440
0076 820REM
0077 830REM RETRIEVE CONFIG TABLE POWER
0078 840CALLGTPWR(P4)
0079 850REM
0080 860REM =====
0081 870REM PARAMETER RECOVERY
0082 880REM -----
0083 890REM
0084 900LET P=-ABS(P4)
0085 910REM
0086 920CALLRDBIT(36,8,G)
0087 930IF (G=1)GOTO 970
0088 940PRINT "STDN HI-PWR MODE"
00 950PRINT @L8;" STDN HI-PWR MODE"
0090 960GOTO 1060
0091 970CALLRDBIT(36,9,G)
0092 980IF (G=1)GOTO 1030
0093 990LET G=G+1
0094 1000PRINT "TDRS MODE"
0095 1010PRINT @L8;" TDRS MODE"
0096 1020GOTO 1060
0097 1030LET E1=-902
0098 1040GOTO 3440
0099 1050REM
0100 1060CALLRDBIT(36,1,F)
0101 1070IF (F=0)PRINT "FREQ LO"
0102 1080IF (F=0)PRINT @L8;" FREQ LO"
0103 1090IF (F=1)PRINT "FREQ HI"
0104 1100IF (F=1)PRINT @L8;" FREQ HI"
0105 1110PRINT "NOISE BW =" ; B
0106 1120PRINT @L8;" NOISE BW =" ; B
0107 1130PRINT @L8
0108 1140REM
0109 1150REM =====
0110 1160REM LO SETUP & MODE RESET
0111 1170REM -----
0112 1180REM
0113 1190LET E1=CM(61,0)
01 1200IF (E1=0)GOTO 3440
01 1210REM
0116 1220IF (F=1)GOTO 1290
0117 1230LET E1=FB(1,2041,947,916)
0118 1240IF (E1=0)GOTO 3440

```

```

0119 1250LET E1=FQ(2,1841,947,916)
0120 1260IF (E100)GOTO 3440
0121 1270GOTO 1340
0122 1280REM
01 1290LET E1=FQ(1,2106,406,250)
0124 1300IF (E100)GOTO 3440
0125 1310LET E1=FQ(2,1906,406,250)
0126 1320IF (E100)GOTO 3440
0127 1330REM
0128 1340LET E1=AT(2,130)
0129 1350IF (E100)GOTO 3440
0130 1360LET E1=SW(27,0)
0131 1370IF (E100)GOTO 3440
0132 1380LET E1=SW(26,1)
0133 1390IF (E100)GOTO 3440
0134 1400LET E1=SW(44,1)
0135 1410IF (E100)GOTO 3440
0136 1420REM
0137 1430LET E1=PW(-1000)
0138 1440IF (E100)GOTO 3440
0139 1450LET E1=SW(44,1)
0140 1460IF (E100)GOTO 3440
0141 1470REM
0142 1480LET E1=SW(46,0)
0143 1490IF (E100)GOTO 3440
0144 1500LET E1=SW(47,0)
0145 1510IF (E100)GOTO 3440
0146 1520LET E1=SW(48,0)
0147 1530IF (E100)GOTO 3440
0148 1540REM
0. 1550REM SWITCH ASSY CONNECTIONS
0150 1560REM      LH --> FM TX 2
0151 1570REM      UL --> DPLXR HI OR LO
0152 1580FOR K=47 TO 58
0153 1590LET E1=CM(K,0)
0154 1600IF (E100)GOTO 3440
0155 1610NEXT K
0156 1620LET E1=CM(48,1)
0157 1630IF (E100)GOTO 3440
0158 1640LET E1=CM(54,1)
0159 1650IF (E100)GOTO 3440
0160 1660LET E1=CM(55,1)
0161 1670IF (E100)GOTO 3440
0162 1680IF (F=0)LET E1=CM(51,1)
0163 1690IF (E100)GOTO 3440
0164 1700IF (F=1)LET E1=CM(52,1)
0165 1710IF (E100)GOTO 3440
0166 1720REM
0167 1730REM =====
0168 1740REM INSTRUCTION OUTPUT
0169 1750REM -----
0170 1760REM
0171 1770PRINT "CONNECT PREAMP OUTPUT 'J4' TO IDEAL RCVR S-BAND INPUT"
0172 1780PRINT "CONNECT SW ASSY OUTPUT 'J7' TO COUPLED PORT OF 10 DB COUPLER"
0173 1790PRINT "POWER UP 'RF', 'IF', AND 'LO' AMPLIFIERS"
01 1800PRINT "CONNECT IDEAL RCVR 'IF' AMP OUTPUT TO SPECTRUM ANALYZER"
01 1810PRINT "CONNECT IDEAL RCVR 'LO' TO UPLINK SOURCE PORT"
0176 1820REM
0177 1830REM
0178 1840REM =====

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0179 1850REM TUNE 'IF' FILTER
0180 1860REM
0181 1870REM
0182 1880PRINT "CENTER 'RF' & 'IF' FILTERS ON CARRIER AT 200 MHZ"
0183 1890PAUSE
0184 1900LET E1=SW(46,1)
0185 1910IF (E1=0)GOTO 3440
0186 1920LET E1=SW(47,1)
0187 1930IF (E1=0)GOTO 3440
0188 1940LET E1=SW(48,1)
0189 1950IF (E1=0)GOTO 3440
0190 1960REM
0191 1970LET E1=PW(-ABS(P4)+10)
0192 1980IF (E1=0)GOTO 3440
0193 1990LET E1=SW(44,1)
0194 2000IF (E1=0)GOTO 3440
0195 2010REM
0196 2020PRINT "CONNECT IDEAL RCVR 'IF' AMP OUTPUT TO POWER METER EXT PORT"
0197 2030PRINT "DISCONNECT 10 DB COUPLER COUPLED PORT INPUT & TERMINATE"
0198 2040PRINT " 'COUPLER' WITH 50 OHM LOAD"
0199 2050PRINT "DO NOT MAKE ANY POWER METER CALLS WHICH REQUIRE ZEROING"
0200 2060REM
0201 2070PAUSE
0202 2080REM
0203 2090REM =====
0204 2100REM READ PREAMP NOISE LEVEL
0205 2110REM -----
0206 2120REM
0207 2130LET E1=SW(37,1)
0208 2140IF (E1=0)GOTO 3440
0209 2150PRINT "WAIT FOR NOISE LEVEL ON PWR METER TO SETTLE"
0210 2160PAUSE
0211 2170LET E1=PW(1,W,-10)
0212 2180IF (E1=0)GOTO 3440
0213 2190PRINT
0214 2200PRINT "OUTPUT PREAMP NOISE PWR=";W
0215 2210PRINT "LB;" OUTPUT PREAMP NOISE PWR=";W
0216 2220PRINT
0217 2230REM
0218 2240REM =====
0219 2250REM READ 'IF' AMP NOISE FLOOR
0220 2260REM -----
0221 2270REM
0222 2280PRINT "DISCONNECT THRU PORT INPUT "
0223 2290PRINT "TERMINATE COUPLER WITH 50 OHM LOAD"
0224 2300PAUSE
0225 2310REM
0226 2320LET E1=PW(1,Y,-10)
0227 2330IF (E1=0)GOTO 2380
0228 2340IF (E1=0-227)GOTO 3440
0229 2350PRINT "LB;" 'IF' AMP NOISE FLOOR < 70"
0230 2360PRINT " 'IF' AMP NOISE FLOOR < 70"
0231 2370GOTO 2420
0232 2380PRINT "LB;" 'IF' AMP NOISE FLOOR =";Y
0233 2390PRINT " 'IF' AMP NOISE FLOOR =";Y
0234 2400REM
0235 2410REM =====
0236 2420REM READ CS SIGNAL LEVEL
0237 2430REM -----
0238 2440REM

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0239 2450PRINT "RECONNECT COUPLED PORT INPUT "
0240 2460PAUSE
0241 2470REM
0242 2480LET E1=PM(1,S,-10)
0243 2490PRINT #L9;"OUTPUT SIGNAL PWR=",S
0244 2500IF (E1#0)GOTO 3440
0245 2510REM SIGNAL POWER HOMING LOOP
0246 2520FOR K=1TO 30
0247 2530LET E=S-N
0248 2540LET I=-(INT(100+E)/100)
0249 2550IF (ABS(I)=0)GOTO 2640
0250 2560LET P=P+I
0251 2570PRINT #L9;" SIGNAL INC=";I,"INPUT SIGNAL PWR=";P
0252 2580LET E1=AT3AD(-I)
0253 2590IF (E1#0)GOTO 3440
0254 2600LET E1=PM(1,S,-10)
0255 2610PRINT #L9;"OUTPUT SIGNAL PWR=",S
0256 2620IF (E1#0)GOTO 3440
0257 2630NEXT K
0258 2640REM
0259 2650PRINT "INPUT SIGNAL PWR TO COUPLER =" ;P
0260 2660PRINT #L8;" INPUT SIGNAL PWR TO COUPLER =" ;P
0261 2670PRINT "OUTPUT SIGNAL = " ;S,"NOISE = " ;N
0262 2680PRINT #L8;" OUTPUT SIGNAL PWR = " ;S
0263 2690REM =====
0264 2700REM READ CW SIGNAL + NOISE LEVEL
0265 2710REM
0266 2720PRINT "RE-CONNECT THRU PORT INPUT "
0267 2730PAUSE
0268 2740LET E1=PM(1,T,-10)
0269 2750IF (E1#0)GOTO 3440
0270 2760REM
0271 2770PRINT
0272 2780PRINT "OUTPUT SIGNAL + NOISE = " ;T
0273 2790PRINT #L8;" OUTPUT SIGNAL + NOISE PWR = " ;T
0274 2800PRINT #L8
0275 2810PRINT
0276 2820REM
0277 2830REM =====
0278 2840REM RESET PWR
0279 2850REM -----
0280 2860REM
0281 2870PRINT "TERMINATE POWER METER EXTERNAL PORT"
0282 2880PAUSE
0283 2890REM
0284 2900LET E1=SW(46,0)
0285 2910IF (E1#0)GOTO 3440
0286 2920LET E1=SW(47,0)
0287 2930IF (E1#0)GOTO 3440
0288 2940LET E1=SW(48,0)
0289 2950IF (E1#0)GOTO 3440
0290 2960REM
0291 2970LET P=R
0292 2980LET E1=PM(P,10)
0293 2990IF (E1#0)GOTO 3440
0294 3000LET E1=SW(44,1)
0295 3010IF (E1#0)GOTO 3440
0296 3020REM
0297 3030PRINT "RECONNECT 'IF' OUTPUT TO PWR METER EXTERNAL PORT"
0298 3040PAUSE

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0299 3050REM
0300 3060REM
0301 3070LET E1=SW(37,1)
0302 3080IF (E100)GOTO 3440
0303 3090LET E1=PM(1,X,-10)
0304 3100IF (E100)GOTO 3440
0305 3110PRINT 0L9;"OUTPUT PWR=";X
0306 3120REM
0307 3130REM SIGNAL POWER HOMING LOOP
0308 3140FOR K=1TO 30
0309 3150LET E=X-T
0310 3160LET I=-(INT(100+E)/100)
0311 3170IF (ABS(I)=0)GOTO 3260
0312 3180LET P=P+I
0313 3190PRINT 0L9;" SIGNAL INC=";I;"INPUT SIGNAL PWR=";P
0314 3200LET E1=AT3AD(-I)
0315 3210IF (E100)GOTO 3440
0316 3220LET E1=PM(1,X,-10)
0317 3230PRINT 0L9;"OUTPUT PWR=";X
0318 3240IF (E100)GOTO 3440
0319 3250NEXT K
0320 3260REM
0321 3270PRINT
0322 3280PRINT "INPUT SIGNAL PWR TO PREAMP =" ;P
0323 3290PRINT 0L8;" INPUT SIGNAL PWR TO PREAMP =" ;P
0324 3300PRINT "OUTPUT POWERS = " ;X,T
0325 3310PRINT 0L8;" OUTPUT SIGNAL + NOISE PWR = " ;X
0326 3320PRINT 0L8
0327 3330REM
0328 3340LET E1=AT(1,-1300)
0329 3350IF (E100)GOTO 3440
0330 3360LET E1=AT(2,-1300)
0331 3370IF (E100)GOTO 3440
0332 3380LET E1=SW(27,1)
0333 3390IF (E100)GOTO 3440
0334 3400REM
0335 3410REM
0336 3420STOP
0337 3430REM ~~~~~
0338 3440REM ERROR HANDLING ROUTINE
0339 3450REM
0340 3460PRINT 0L9;"ERROR",E1
0341 3470LET E3=ERRCK(E1)
0342 3480LET E1=0
0343 3490STOP
0344 3500REM
0345 3510REM ~~~~~
0346 3520REM ~~~~~
0347 3530REM VARIABLE DEFINITIONS
0348 3540REM
0349 3550REM B = NOISE BANDWIDTH IN DB
0350 3560REM E = POWER LEVEL ERROR
0351 3570REM E1 = ERROR RETURN CODE
0352 3580REM F = HI-LO FREQ INDEX
0353 3590REM G = SGLS OR TORS-STDN MODE INDEX
0354 3600REM I = POWER INCREMENT BY PIN DIODE ATTENUATOR
0355 3610REM K = LOOP INDEX
0356 3620REM (L8)= HARDCOPY LIST LU 8
0357 3630REM (L9)= DEBUG LIST LU 9
0358 3640REM W = INPUT NOISE POWER

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0359 3650REM P = INPUT SIGNAL POWER
0360 3660REM P1 = CONSOLE LU # FOR INSTRUCTION OUTPUT
0361 3670REM P2 = UUT CONFIGURATION # FOR C/N0 TEST - TEST SETUP BYPASS
0362 3680REM P3 = UNUSED PARAM
0363 3690REM P4 = INPUT SIGNAL POWER FOR C/N0 - TRUE VALUE IN DBM
0364 3700REM R = PWR RESET VALUE
0365 3710REM T = SIGNAL + NOISE OUTPUT PWR
0366 3720REM X = SIGNAL + NOISE OUTPUT PWR
0367 3730REM " = '1F' AMP NOISE FLOOR
0368 3740END

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0059 590PRINT
0060 600PRINT
0061 610PRINT "3) REMOVE FR
0062 620PRINT " EXT POWER
0063 630PAUSE
0064 640REM *****
0065 650REM P1=NOISE LEVEL
0066 660REM P2=NOISE+SIGNAL
0067 670REM P3=NOISE +3.0 DB
0068 680REM
0069 690LET I=SW(49,1)
0070 700LET I=SW(37,1)
0071 710LET I=PW(1,P1,-10)
0072 720LET D3=0
0073 730REM *****
0074 740LET I=SW(49,0)
0075 750LET M=0
0076 760LET I=PW(1,P2,-10)
0077 770LET P3=P1+3
0078 780IF ABS(P2-P3) < 0.1 THEN
0079 790LET D1=-(P3-P2)
0080 800LET D2=D1/2
0081 810LET D3=D2+D3
0082 820LET D4=-D3+10
0083 830LET D5=L1+D4
0084 840LET I=AT3AD(D2)
0085 850PRINT " "
0086 860GOTO 760
0087 870REM BASIC TIME DATE C
0088 880LET D9=TIM(2)
0089 890FOR M9=1 TO 12
0090 900LET S9=31
0091 910IF (M9=2) LET S9=26
0092 920IF (M9=4 OR M9=6 OR M9=
0093 930IF (D9< S9) GOTO 933
0094 940LET D9=D9-S9
0095 950NEXT M9
0096 960PRINT " DATE =" M9 "
0097 970PRINT "6:" DATE =" M9
0098 980PRINT " IDEAL RX C
0099 990PRINT "6:" IDEAL R
0100 1000PRINT " METHOD:

CH0 T=00004 IS ON C00002 USING 00012 BLKS R=0016

0001 10REM
0002 20REM IDEAL RECEIVER C/HO CONFIGURATION PP
0003 30REM F YEE
0004 40REM
0005 50REM TABLES BP, MH
0006 60REM
0007 70LET P2=GTPAR(2)
0008 80REM
0009 90REM
0010 100REM P2=UIT CONFIGURATION 0
0011 110REM P2=NEGATIVE TEST SET BYPASS
0012 120REM P2=9999 UIT BYPASS
0013 130REM
0014 140IF (P2<0) GOTO 710
0015 150IF (P2=9999) GOTO 180
0016 160REM LET E1=CF(ABS(P2))
0017 170REM ***** LO FOR IDEAL RX AT
0018 180LET I=SW(27,0)
0019 190LET I=SW(26,1)
0020 200LET I=SW(44,1)
0021 210REM READ UIT FREQ MODE B1=0 =FREQ
0022 220CALL RDBIT(36,1,B1)
0023 230REM READ UIT MODE SGLS/TDRSS B2=0 =SGL
0024 240CALL RDBIT(36,9,B2)
0025 250IF B1=1 AND B2=1 GOTO 290
0026 260IF B1=0 AND B2=1 GOTO 320
0027 270IF B1=1 AND B2=0 GOTO 350
0028 280IF B1=0 AND B2=0 GOTO 380
0029 290LET A=1906
0030 300LET B=406
0031 310GOTO 410
0032 320LET A=1841
0033 330LET B=947
0034 340GOTO 410
0035 350LET A=1631
0036 360LET B=787
0037 370GOTO 410
0038 380LET A=1575
0039 390LET B=733
0040 400REM MODES SGLS, STDN, STDN LO, TDRSS
0041 410LET I=FG(2,A,B,0)
0042 420LET I=AT(2,130)
0043 430REM ***** SET RF INPUT TO IDE
0044 440PRINT " TERMINATE EXT POWER METER INTO
0045 450PAUSE
0046 460PRINT " "
0047 470LET L1=-990
0048 480LET I=PW(L1)
0049 490LET I=SW(44,1)
0050 500REM
0051 510PRINT "1) BREAK IF OUTPUT OF FIRST MIXER
0052 520PRINT " SPECTRUM ANALYZER AND TUNE S-B-
0053 530PRINT " 238 +-50 MHZ AND RECONNECT AND
0054 540PRINT " "
0055 550PRINT " "
0056 560PRINT "2) BREAK IF OUTPUT OF 2ND HP 8447
0057 570PRINT " ANALYZER AND TUNE NOISE FILTER
0058 580PRINT " SYMMETRICAL RESPONSE"

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0059 590PRINT
0060 600PRINT
0061 610PRINT "3) REMOVE FROM ANALYZER AND CONNECT TO "
007 620PRINT " EXT POWER METER J10 THEN TYPE GO"
008 630PAUSE
0064 640REM ***** MEASURE NOISE WITH PM *****
0065 650REM P1=NOISE LEVEL
0066 660REM P2=NOISE+ SIGNAL
0067 670REM P3=NOISE +3.0 DB
0068 680REM
0069 690LET I=SW(49,1)
0070 700LET I=SW(37,1)
0071 710LET I=PM(1,P1,-10)
0072 720LET D3=0
0073 730REM ***** MEASURE SIGNAL WITH PM *****
0074 740LET I=SW(49,0)
0075 750LET M=0
0076 760LET I=PM(1,P2,-10)
0077 770LET P3=P1+3
0078 780IF ABS(P2-P3)<.01 THEN 980
0079 790LET D1=-(P3-P2)
0080 800LET D2=D1/2
0081 810LET D3=D2+D3
0082 820LET D4=-D3+10
0083 830LET D5=L1+D4
0084 840LET I=AT3AD(D2)
0085 850PRINT " "
0086 860GOTO 760
0087 870REM BASIC TIME DATE CONVERSION & PRINTOUT
0088 880LET D9=TIM(2)
0089 890FOR M9=1 TO 12
0090 900LET S9=31
0091 910IF (M9=2) LET S9=26
0092 920IF (M9=4 OR M9=6 OR M9=9 OR M9=11) LET S9=30
0093 930IF (D9<= S9) GOTO 933
0094 940LET D9=D9-S9
0095 950NEXT M9
0096 960PRINT " DATE =":M9:"/" :D9:"/" :TIM(3) : "TIME =":TIM(1) : ":" :TIM(0)
0097 970PRINT 66: "DATE =":M9:"/" :D9:"/" :TIM(3) : "TIME =":TIM(1) : ":" :TIM(0)
0098 980PRINT " IDEAL RX C/N0 MEASUREMENT"
0099 990PRINT 66: " IDEAL RX C/N0 MEASUREMENT"
0100 1000PRINT " METHOD: SIGNAL INCREMENTED TO 3.00+- .01DB ABOVE NOISE"

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